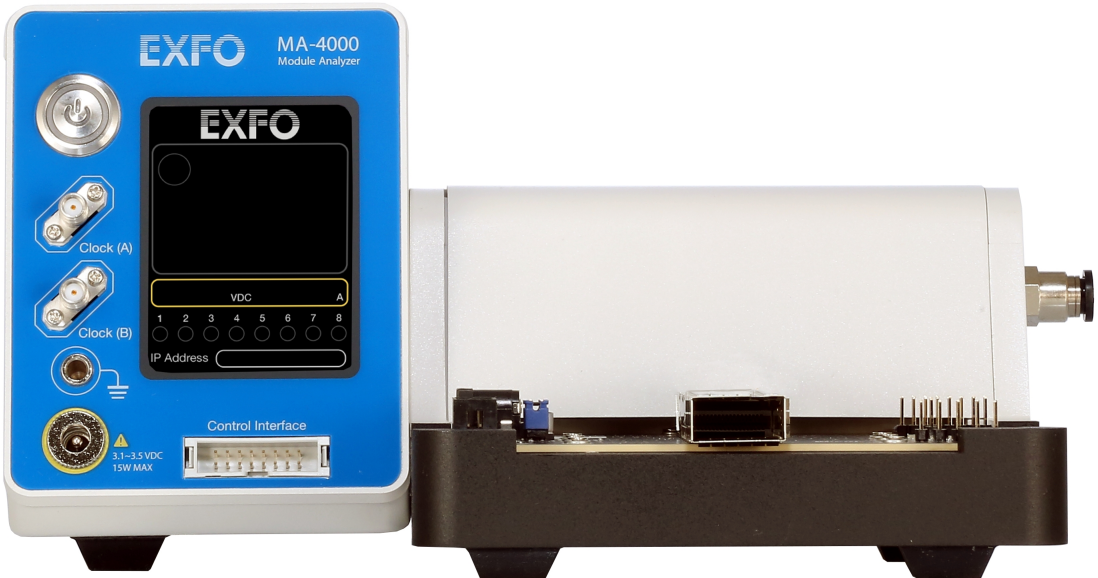


MA-4000

Module Analyzer



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Units of Measurement

Units of measurement in this publication conform to SI standards and practices.

Patents

The exhaustive list of patents is available at EXFO.com/patent.

Version number: 1.0.0.1

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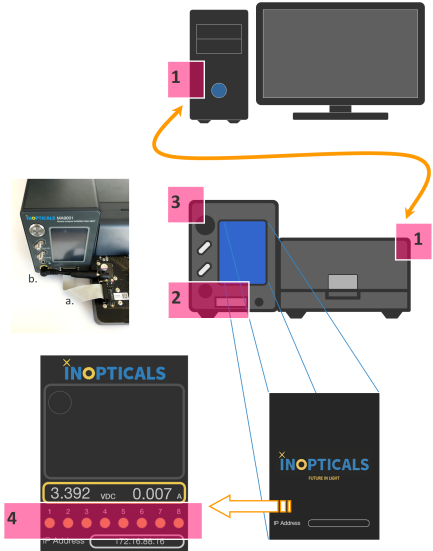
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1 6 Steps to Measure BER

Step 1: Hardware Configuration

To power on the unit:

1. Connect the Ethernet cable from the control PC to the RJ45 port on the rear of the chassis.
2. Connect the cables on the front panel:
 - 2a. Flat flexible cable for control interface
 - 2b. Short power cord for module board
3. Push power button on the front panel.
4. Wait for initialization which is done when the IP appears on the chassis screen and the 8 LEDs turn yellow.



Note: If the IP address does not appear after 5 min, it means the unit is not connected to an Ethernet device yet. Please check the Ethernet cable and RJ45 port on the PC.

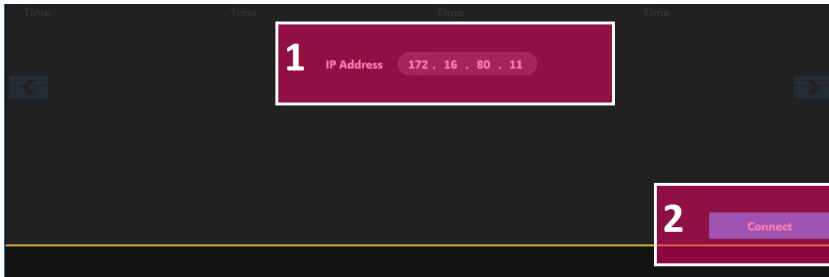
6 Steps to Measure BER

Step 2: Link to Module Analyzer

Step 2: Link to Module Analyzer

To link to the MA (Module Analyzer):

1. Input the **IP address** of the MA into the GUI, for example: 172.16.80.11.
(An example of IP of control PC = 172.16.1.10, and subnet mask = 255.255.0.0.)



Note: The IP address is shown on the chassis screen when initialization is completed.

2. Click **Connect** button to enter the main control page.

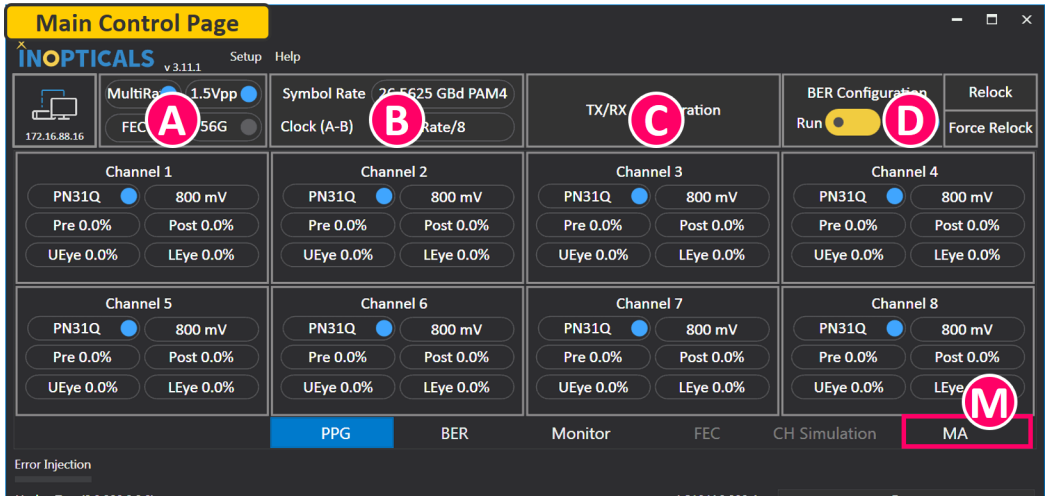
There are 4 main areas plus 1 page to give you the whole control of the MA:

- A – Function Mode
- B – Modulation and Symbol Rate
- C – TX/RX Configuration

6 Steps to Measure BER

Step 2: Link to Module Analyzer

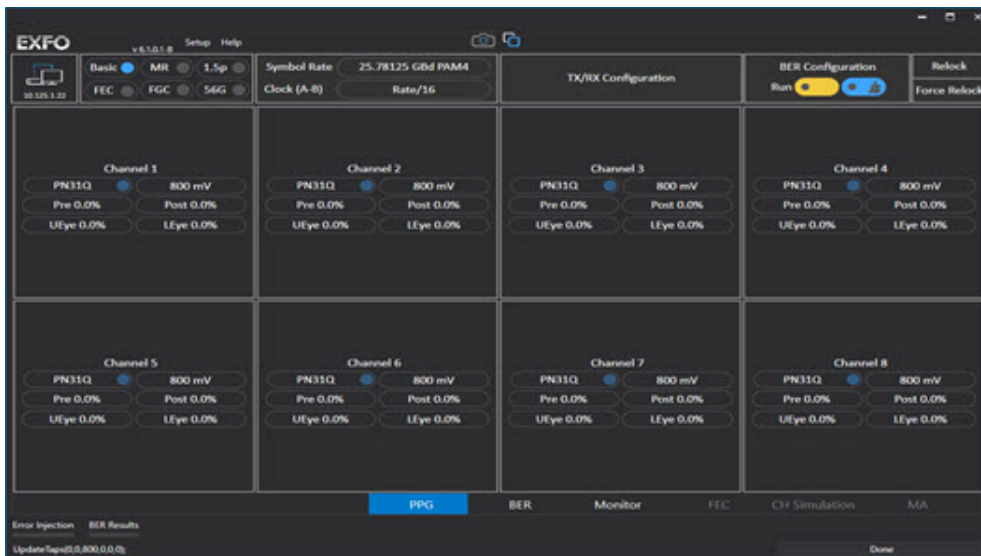
- D – BER Test Method
- M – Module Test Board (optional)



6 Steps to Measure BER

Step 3: Main Control Page

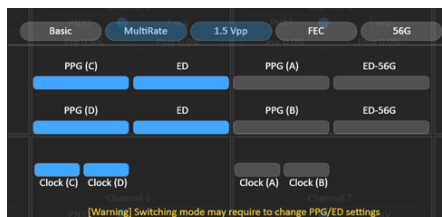
Step 3: Main Control Page



Function Mode

Click the Function Mode area (top-left side) of the main control page, to select the following options (dependent on purchased options):

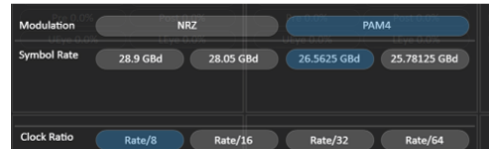
- **MultiRate** (default mode)
- **1.5 Vpp** (default mode)
- **FEC** (option) enables FEC simulator.



Modulation and Symbol Rate

Clicking this area (second from left on the top of the control page) allows you to set the following items:

- **Modulation**
- **Symbol Rate**
- **Clock Ratio**



Note: When selecting *Clock Ratio Rate/8* and *Symbol Rate 26.5625 GBd*, the output clock freq is 3.32 GHz.

6 Steps to Measure BER

Step 4: TX/RX Settings

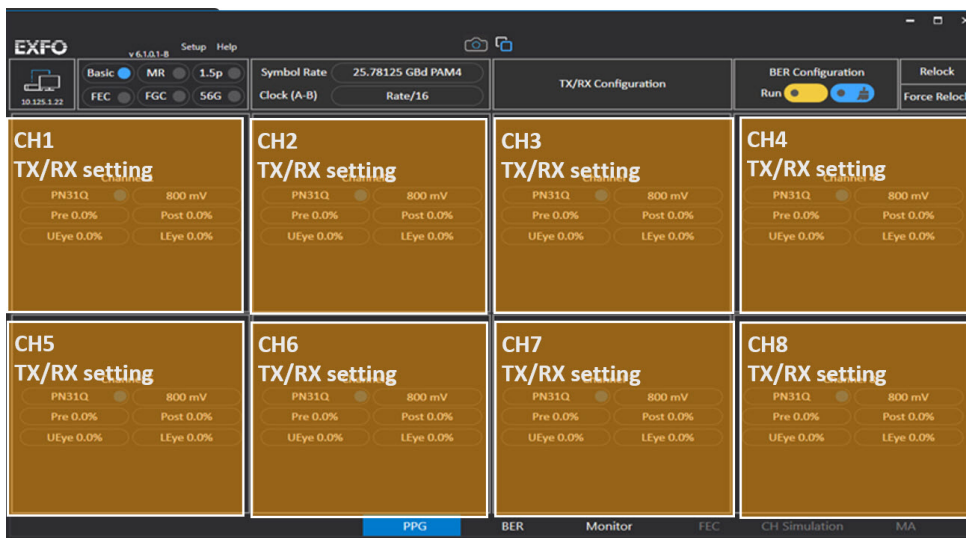
Step 4: TX/RX Settings

Clicking this area (third from right on the top of the control page) allows you to set the TX/RX configuration of all channels, as follows:

- Test Pattern
- Amplitude
- Pre/Post-Cursor
- Upper/Lower Eye (PAM4 only)
- RX Polarity
- RX Sensitivity
- CTLE



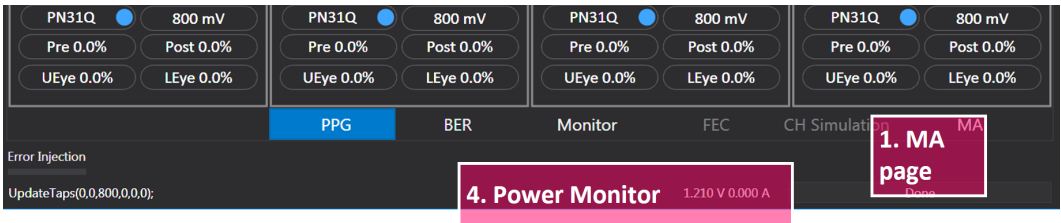
Note: Click on a channel to pop up an individual channel setting window.



Step 5: Module Test Board Settings

To configure the module test board:

1. From the main control page, click the **MA** page.



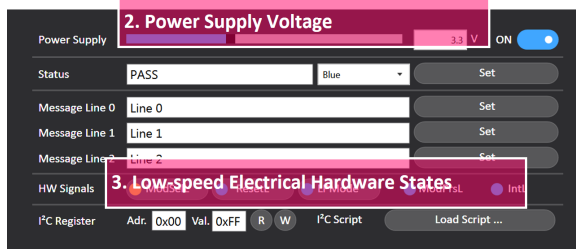
2. Set the **Power Supply** voltage for TRX module and turn it **ON**, for example 3.3 V.

3. Click **HW Signals** buttons to switch High/Low states, for example: **ModSelL**, **ResetL**, **LPMODE**.

4. Check the true values on TRX.

4a. Plug TRX into the module test board.

4b. Read the voltage and current from the power monitor bar.



Note: The MA page is valid, when the following 2 cables are connected:

Board power
Control interface



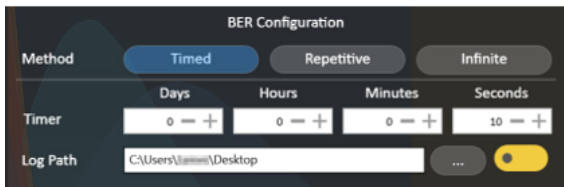
6 Steps to Measure BER

Step 6: BER Test Page

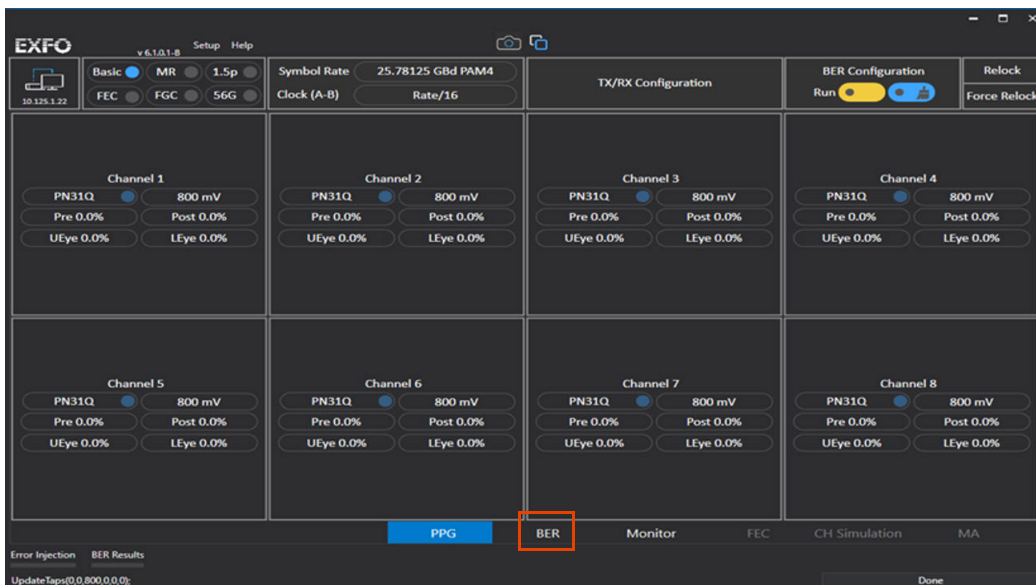
Step 6: BER Test Page

To setup how to test the BER (bit error rate) of all channels:

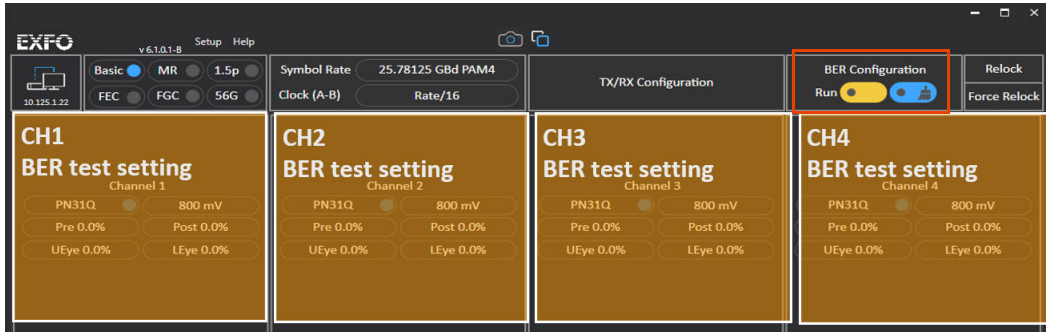
1. Click **BER Configuration** from the top-right side of the main control page.



2. Click the **BER** tab to show BER test page.



3. Switch on BER test to run the test.

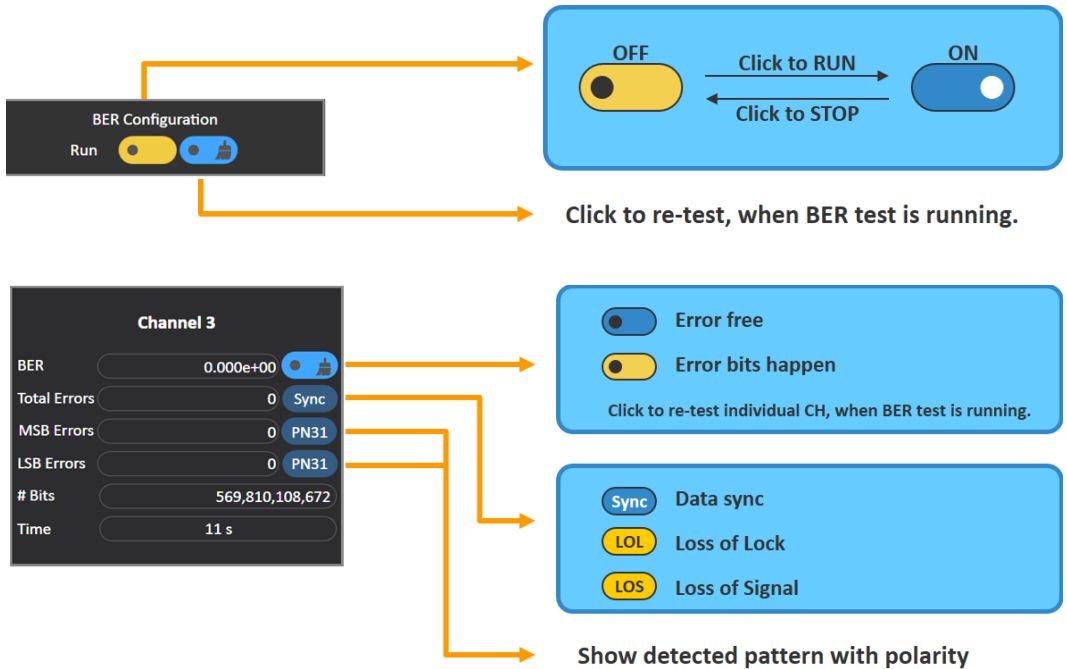


4. Click on a channel area to pop up an individual channel setting window.

2 GUI Indication

BER Test Page

Switch and LED Indicators



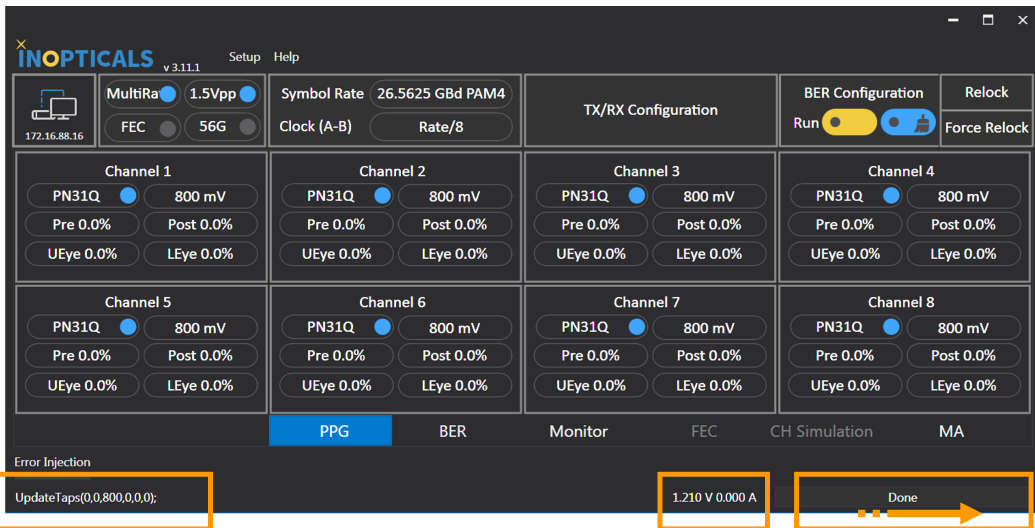
GUI Indication

API Command and Progress Bar Status Info

API Command and Progress Bar Status Info

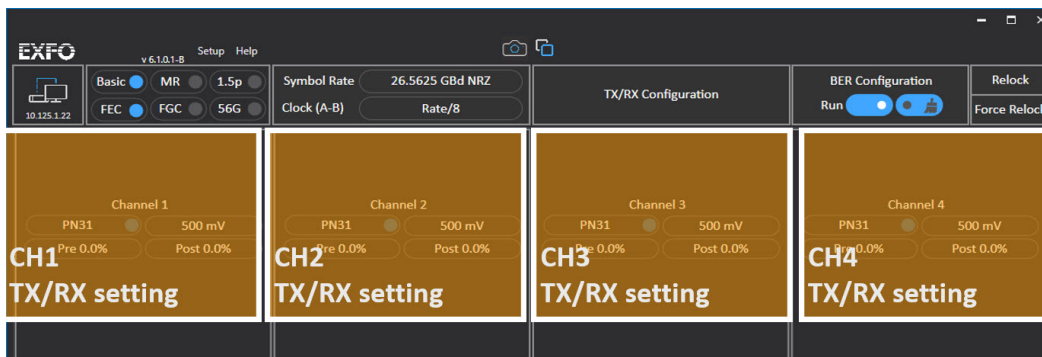
The following information is displayed on the main control page:

- The bottom left displays corresponding API command information during the process, for ease of use.
- Power **Monitor** shows the voltage and current at Vcc of the module test board.
- The bottom-right progress bar displays the **MA** status information including whether or not the process is **Done**.

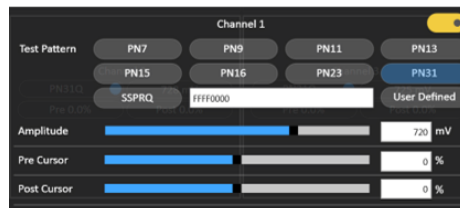


Channel ON/OFF Switch

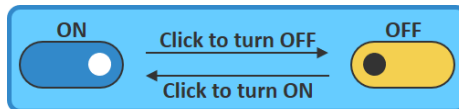
The PPG page allows you to switch individual channels on/off.



Click an individual channel box to enter its PPG setting window.



The switch is in the upper-right corner.



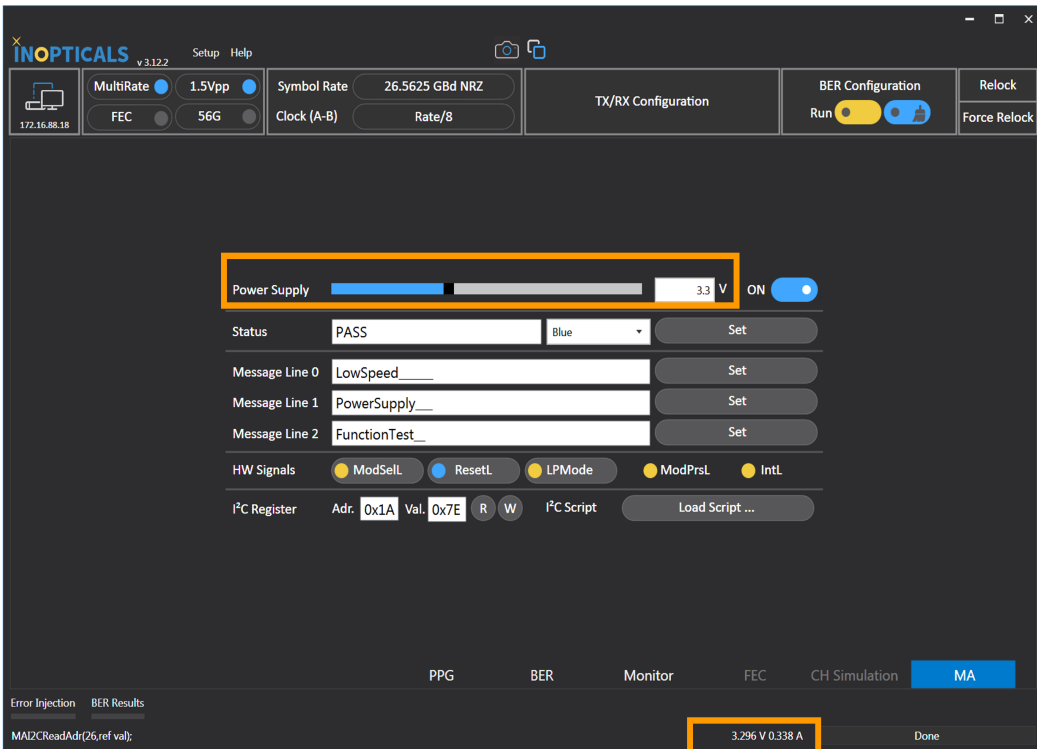
MA Specific Page

Voltage

To set and read the voltage;

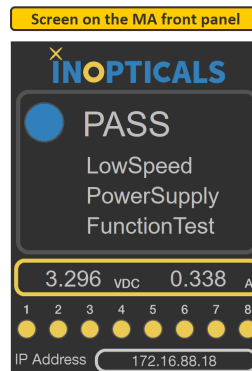
1. Set the voltage generated from **Power Supply**.
2. Using the MA GUI on your PC, click the **Power Supply** switch to turn it on.

MA GUI on PC



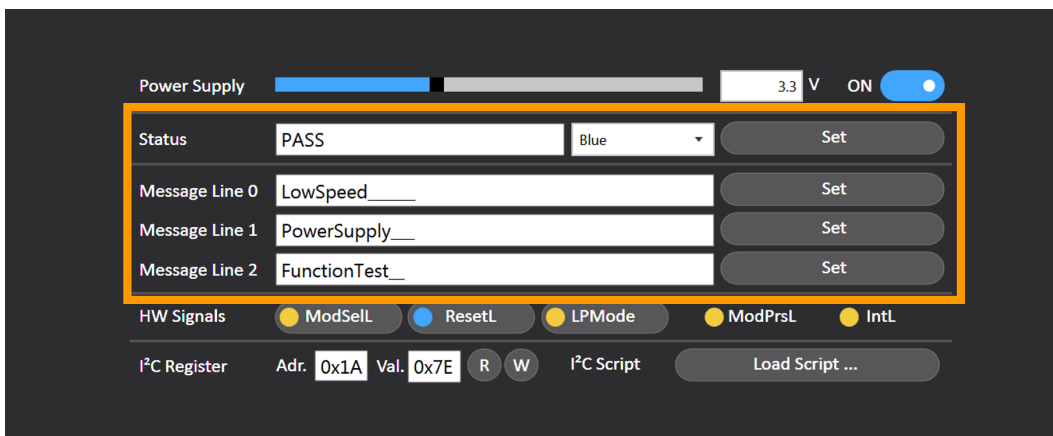
The power **Monitor** shows the voltage and current at Vcc of the module test board. Voltage is decreased due to cable loss and other path loss.

The same information is displayed on the MA front panel screen.



Setting Messages

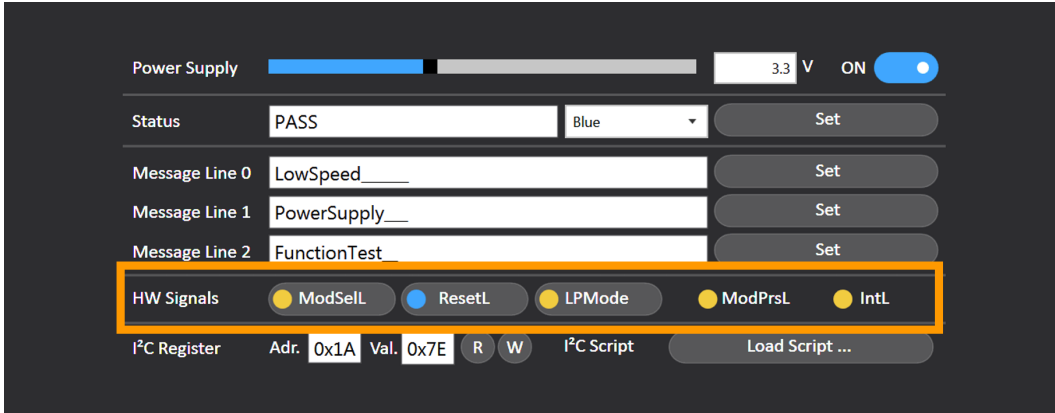
Set the messages to be displayed on the screen of the MA front panel.



GUI Indication

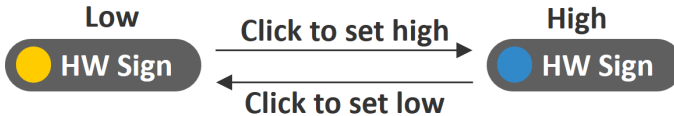
MA Specific Page

Low Speed Signals



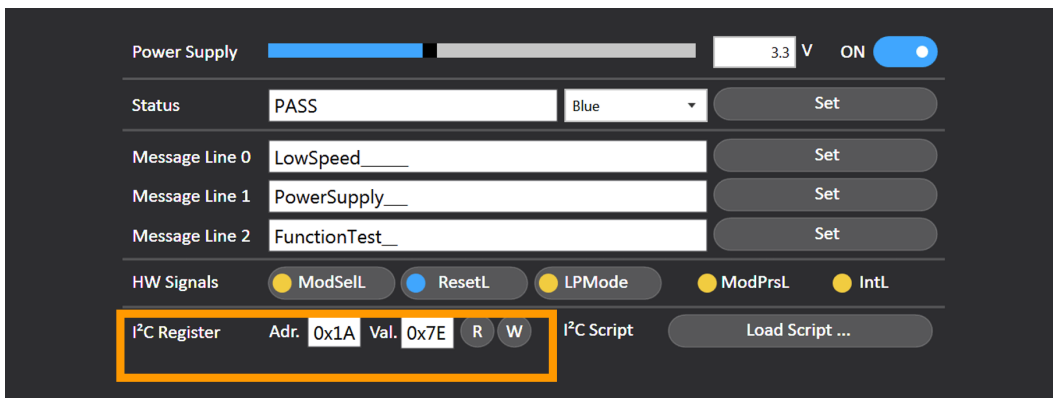
Low speed electrical hardware states are as follows:

- **ModSelL**
- **ResetL**
- **LPMode**
- **ModPrsL** (read only)
- **IntL** (read only)



Quick Access to I²C Register

I²C Control - I²C Register Read (R)/Write (W)



To read Single Byte in the I²C Register:

1. Type the address in Hex¹ in the **Adr.** blank.
2. Click the **R** button.
3. Read the value from **Val.**

To write Single Byte:

1. Type address in Hex in the **Adr.** blank.
2. Type the value in Hex in the **Val.** blank
3. Click the **W** button.

1. hexadecimal

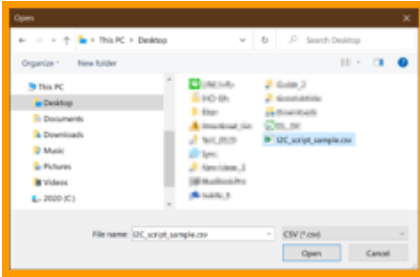
GUI Indication

MA Specific Page

Multiple Access to I²C Register

To load a script to access I²C registers systematically:

1. Click the **Load Script** button.
2. Select a script file. The extension of script file must be CSV.



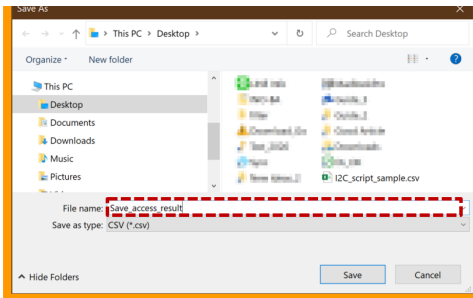
Example of script

```
W, 126, 1  
R, 126, 0  
W, 126, 2  
R, 126, 0  
W, 126, 3  
R, 126, 0
```

- Format of script – Read
R, [address in Dec¹], 0
- Format of script – Write
W, [address in Dec], [value in Dec]

The MA starts to access I²C registers from the TRX module. It takes < 5 sec before a pop up a window allows you to save the result.

3. Type a file name to save the access result.



Example of access result

```
W, 126, 1  
R, 126, 1  
W, 126, 2  
R, 126, 2  
W, 126, 3  
R, 126, 3
```

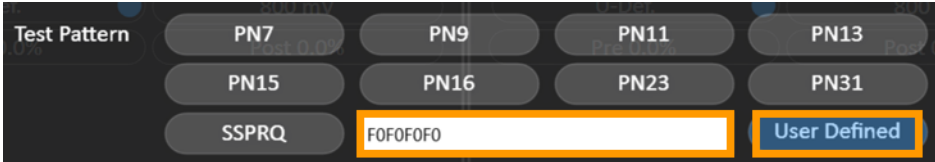
1. decimal

3 Advanced Guide

User Defined Test Pattern

To set the User Defined pattern as Clock:

1. Customize the pattern.
2. Click User Defined.



The **User Defined** pattern is always treated as NRZ, no matter what the data modulation is. Pattern length is 32-bit. Therefore, you can always get **/2 Clock Pattern** by $AAAAAAAA_{\text{hex}}$.

$$[\text{Clock Pattern Frequency}] = [\text{Symbol Rate}] \times [\text{Clock Ratio}]$$

For example:

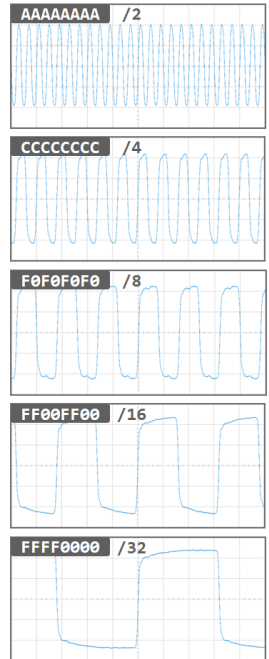
Symbol Rate = 26.5625 GBd

Clock Ratio = /8 ($F0F0F0F0_{\text{hex}}$)

Clock Frequency = 3.32 GHz

Clock Ratio	Clock Pattern*
/2	AAAA AAAA
/4	CCCC CCCC
/8	F0F0 F0F0
/16	FF00 FF00
/32	FFFF 0000

* Length of User Defined Pattern
= 32-bit long
= hex

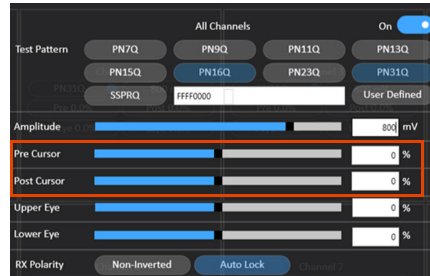


Tuning Emphasis

Pre/Post Cursor

When tuning **Pre Cursor** and **Post Cursor** on GUI, both are normalized, calibrated, and shown as a percentage from -100 % to +100 %.

The equalization is calculated by the following equation:



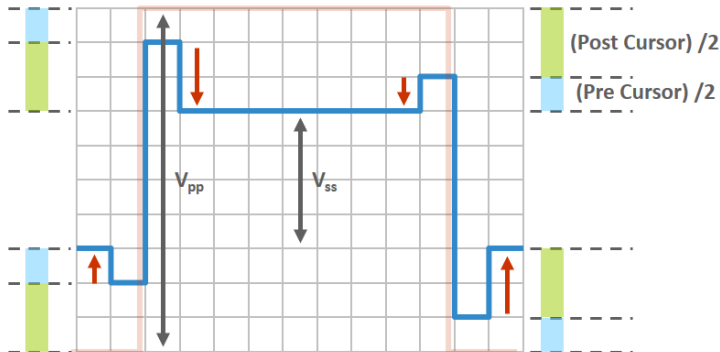
$$20 \times \log_{10} \left[\frac{\text{Amplitude} - (\text{Pre Cursor} + \text{Post Cursor}) \times 1000}{\text{Amplitude} + (\text{Pre Cursor} + \text{Post Cursor}) \times 1000} \right]$$

[Example]

Set Amplitude = 800mV, Pre Cursor = -5%, Post Cursor = -15%

$$\begin{aligned} \text{Then EQ (dB)} &= 20 \times \log \left[\frac{800 - (-0.05 - 0.15) \times 1000}{800 + (-0.05 - 0.15) \times 1000} \right] \\ &= 20 \times \log [1000/600] = \underline{4.4 \text{ (dB)}} \end{aligned}$$

The general definitions are displayed in the following:

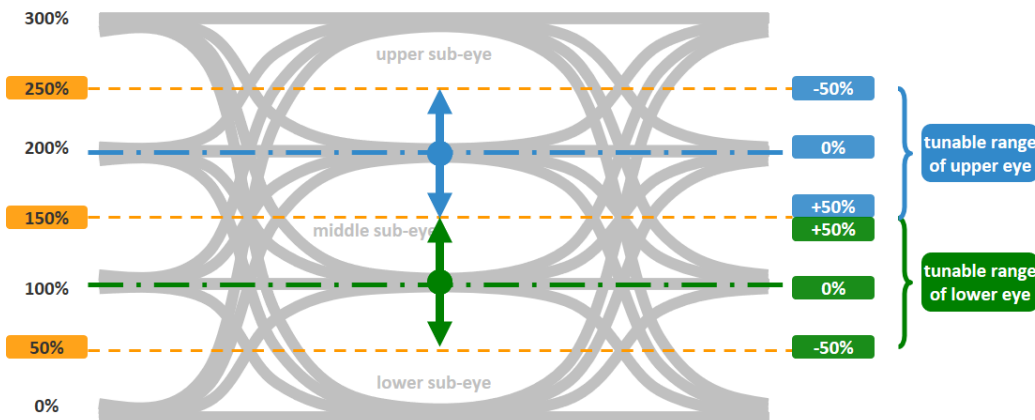
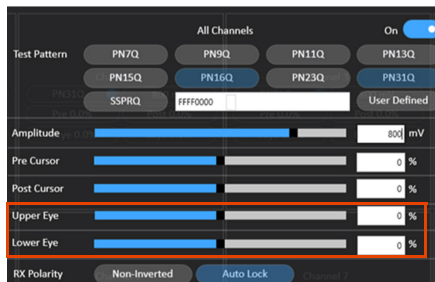


Sub-Eye Heights

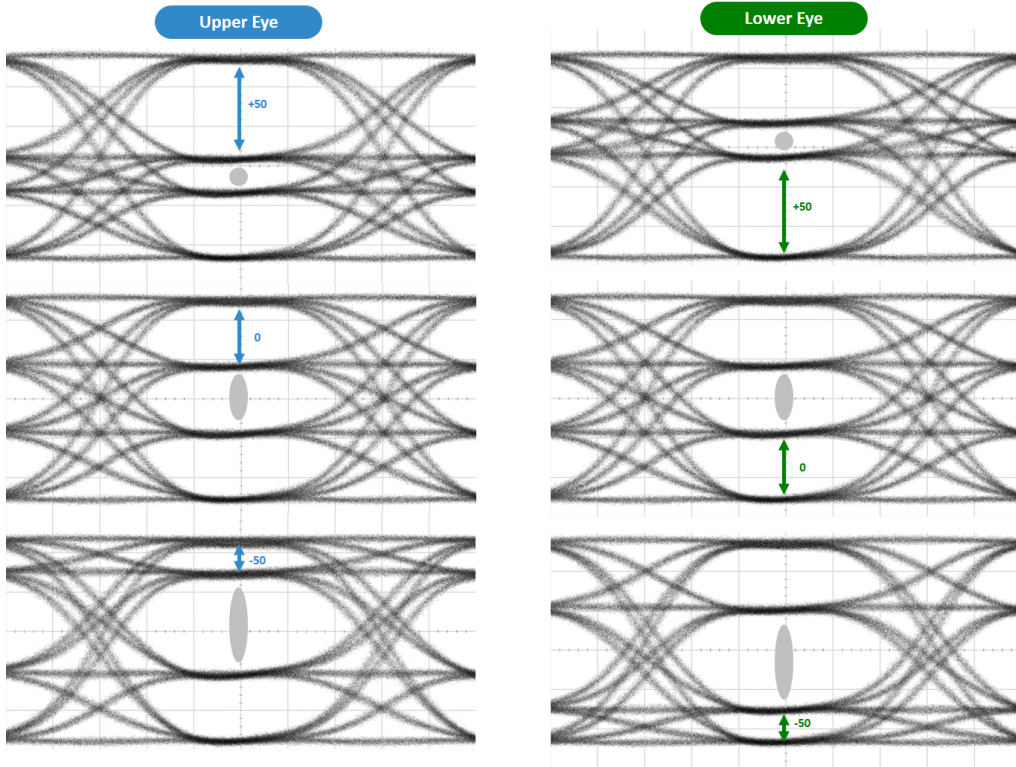
Upper Eye = Upper Sub-eye Height

Lower Eye = Lower Sub-eye Height

To enlarge sub-eye heights, increase the percentage when tuning. Both ranges of **Upper Eye** and **Lower Eye** are from -50 % to +50 %.



Sub-Eye Heights (cont'd)



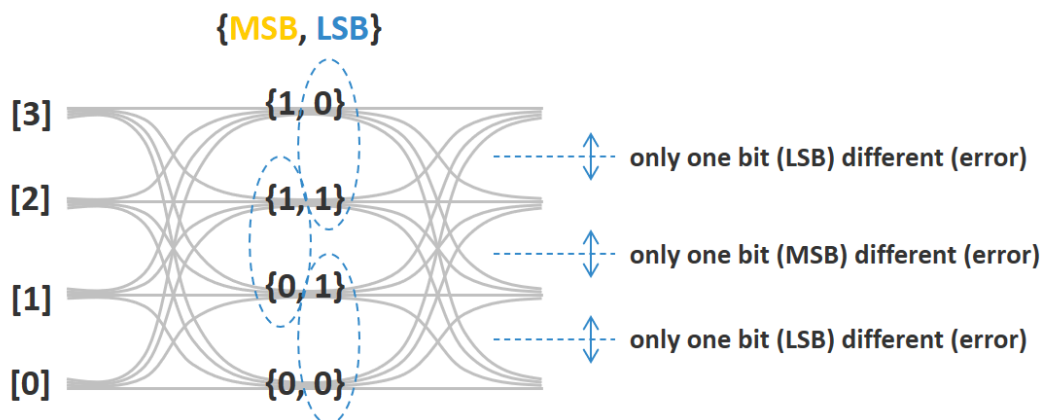
MSB and LSB Errors

The details of **MSB/LSB Errors** are as follows:

- The PAM4 symbol maps to MSB, LSB.
 - MSB = Most Significant Bit
 - LSB = Least Significant Bit
 - **Total Errors = MSB Errors + LSB Errors**
- Better level linearity reduces error bits for both MSB and LSB errors.
- Tuning **Upper/Lower Eye** achieves better linearity.

Channel 4	
BER	4.902e-09
Total Errors	5,209 Sync
MSB Errors	1,126 PN31
LSB Errors	4,083 PN31
# Bits	1,062,634,080,640
Time	20 s

Gray-coded Symbol



Advanced Guide

Selecting the Correct Mode of RX Sensitivity

To achieve better receiving performance, there are 3 modes of **RX Sensitivity** to select:

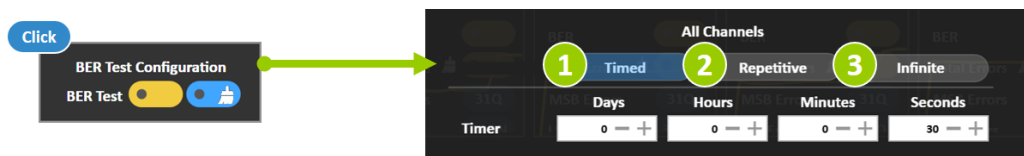
- **High Sensitivity** when input amplitude is < 150 mV.
- **Optimized** for general cases between 150 mV and 750 mV.
- **High Power** when input amplitude is > 750 mV.



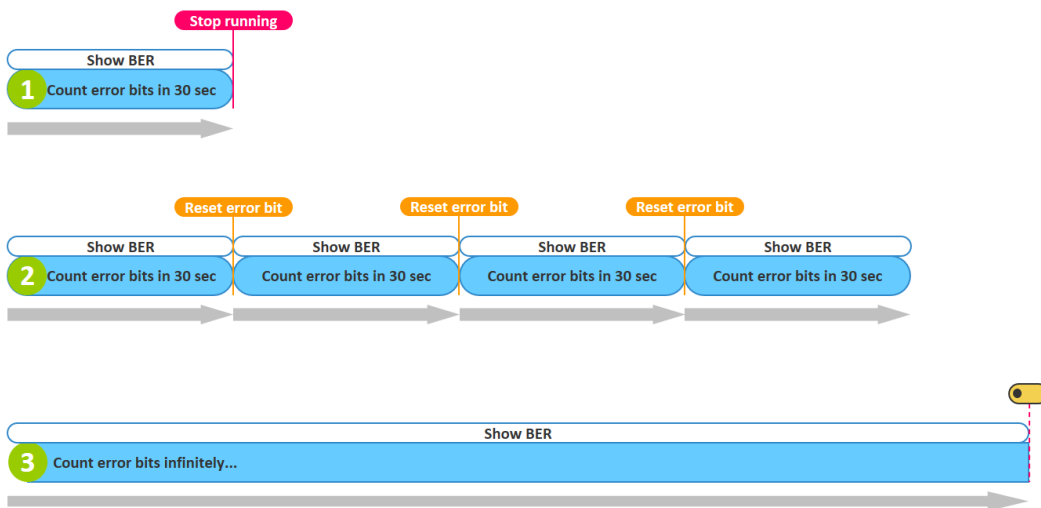
Testing BER

There are 3 methods to test BER:

- **Timed**
- **Repetitive**
- **Infinite**



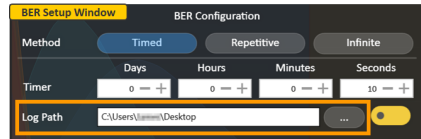
In the example, the **Timer** is set to 30 s.



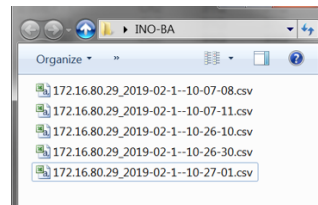
BER Test Results

To automatically log BER test results:

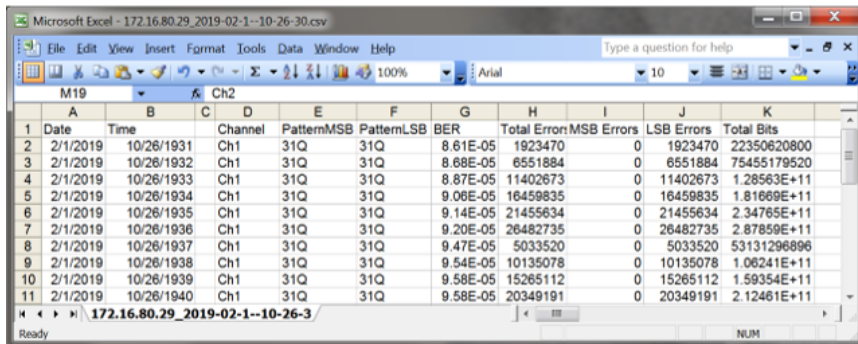
1. In the **Log Path**, enter where to create the folder **INO-BA** and save records.
2. Switch on Auto Log (switch is to the right of the Log Path).



In this example, the auto-saved files are listed in the created folder.



3. Open a file to view the listed BER Test Results.



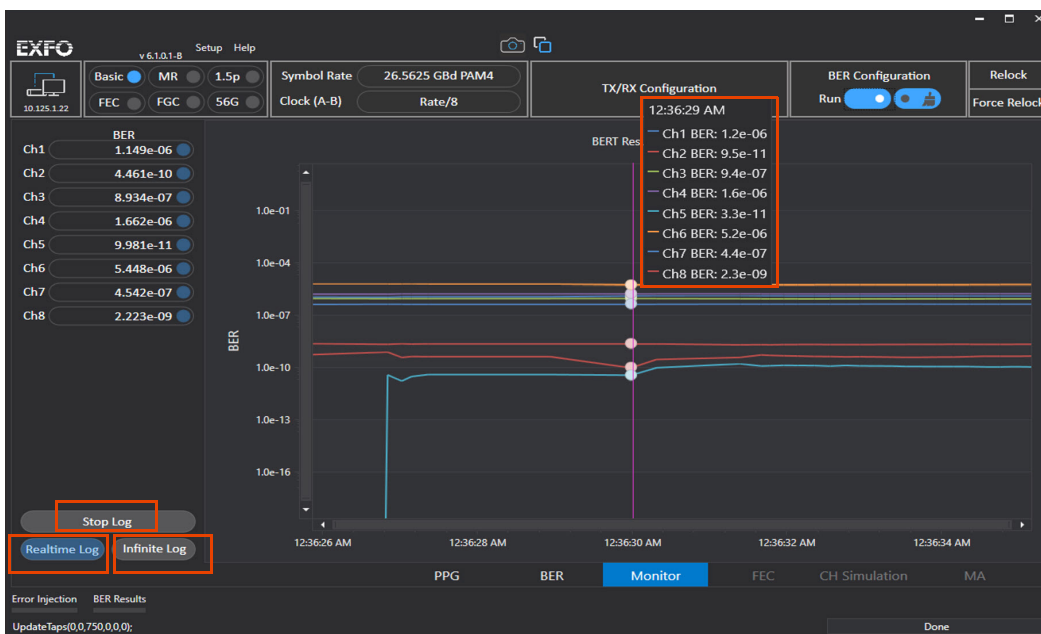
1	Date	Time	Channel	PatternMSB	PatternLSB	BER	Total ErrorMSB	Errors	LSB Errors	Total Bits
2	2/1/2019	10/26/1931	Ch1	31Q	31Q	8.61E-05	1923470	0	1923470	22350620800
3	2/1/2019	10/26/1932	Ch1	31Q	31Q	8.68E-05	6551884	0	6551884	75455179520
4	2/1/2019	10/26/1933	Ch1	31Q	31Q	8.87E-05	11402673	0	11402673	1.28563E+11
5	2/1/2019	10/26/1934	Ch1	31Q	31Q	9.06E-05	18459835	0	18459835	1.81669E+11
6	2/1/2019	10/26/1935	Ch1	31Q	31Q	9.14E-05	21455634	0	21455634	2.34765E+11
7	2/1/2019	10/26/1936	Ch1	31Q	31Q	9.20E-05	26482735	0	26482735	2.87859E+11
8	2/1/2019	10/26/1937	Ch1	31Q	31Q	9.47E-05	5033520	0	5033520	53131296896
9	2/1/2019	10/26/1938	Ch1	31Q	31Q	9.54E-05	10135078	0	10135078	1.06241E+11
10	2/1/2019	10/26/1939	Ch1	31Q	31Q	9.58E-05	15265112	0	15265112	1.59354E+11
11	2/1/2019	10/26/1940	Ch1	31Q	31Q	9.58E-05	20349191	0	20349191	2.12461E+11

BER Monitor Page

BER Monitor visualizes BER versus time, in order to track BER.

To monitor BER:

1. Move your mouse on the plot to show the BER information for all available channels.



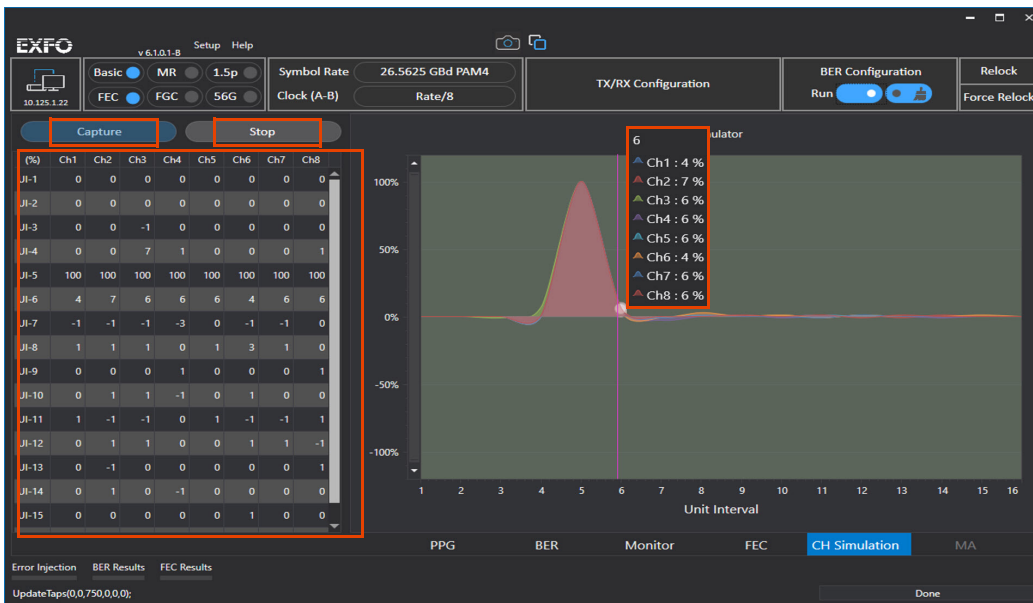
2. Start the **Realtime Log** to plot BER every second.
3. Start the **Infinite Log** to plot BER every 10 s.
4. Stop Logging (**Stop Log**)

CH Simulation Page

CH Simulation allows you to estimate the channel quality by identifying how to compensate channel response.

To start channel simulation:

1. Click **Capture** to get the signal and analyze.
2. Click **Stop** to end the capture.



The CH simulation table displays the normalized response for each UI of every channel.

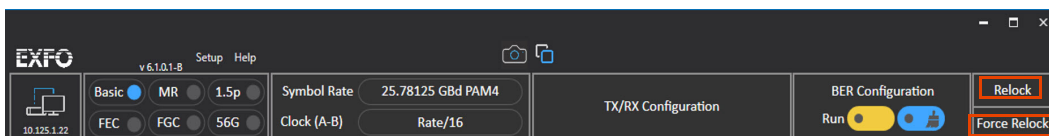
3. Move your mouse on the plot to show the UI response for all available channels.

Relock and Force Relock

Relock is the general function to re-lock the channels which get LOL or poor BER. Perform Relock when a TX signal or channel path is changed.

Note: *When signal quality is marginal, you may need to Relock several times.*

Force Relock is the advanced re-lock function to reset BA and re-lock all channels. This function is more powerful and takes a longer to perform.



4 Error Injection Operation

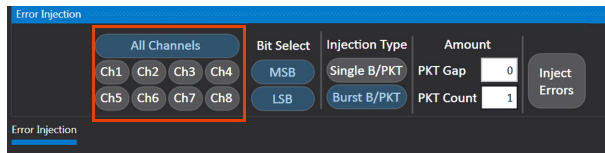
Error Injection Control Panel

To inject errors:

1. Move mouse to lower-left corner of GUI to slide out the **Error Injection** control panel.



2. Select the channel(s) you want errors injected into or select **All Channels**.

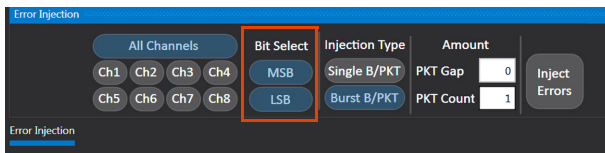


3. Click **Inject Errors** button to generate errors.

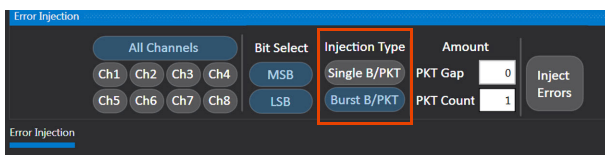
Error Injection Operation

Error Injection Control Panel

- When PAM4 modulation is selected, for **Bit Select**, you can inject errors on **MSB** and/or **LSB**.

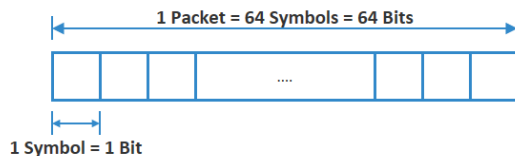


- Define the packet **Injection Type**.

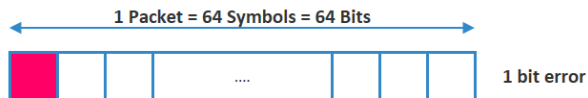


PKT = Packet

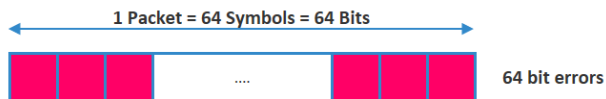
For NRZ:



Single B/PKT



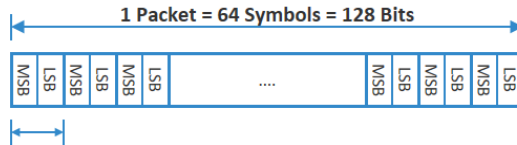
Burst B/PKT



Error Injection Operation

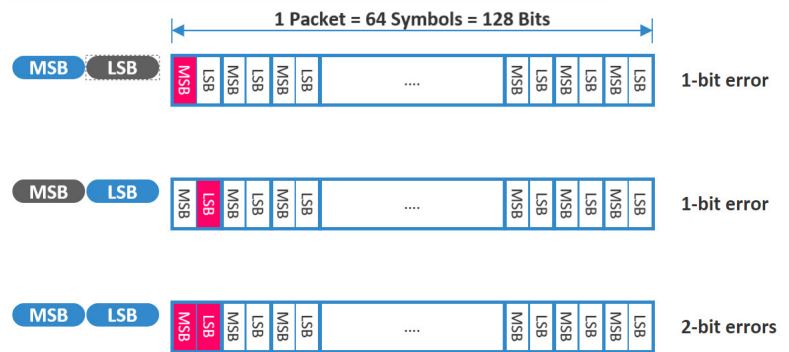
Error Injection Control Panel

For **PAM4**:

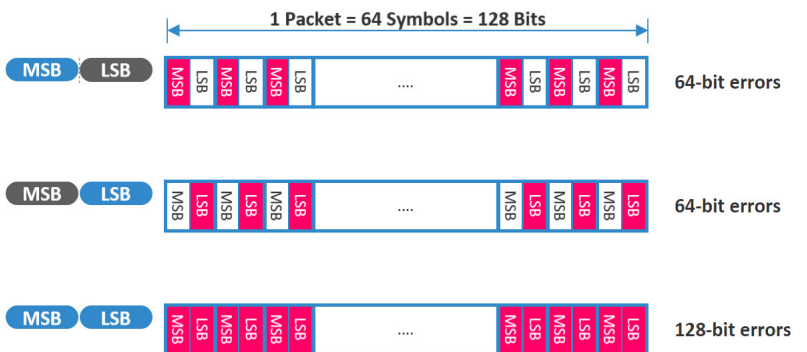


1 PAM4 Symbol

Single B/PKT



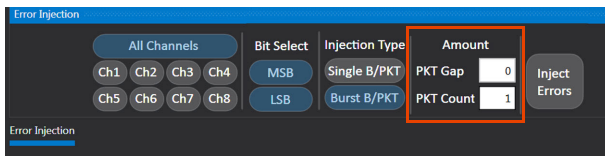
Burst B/PKT



Error Injection Operation

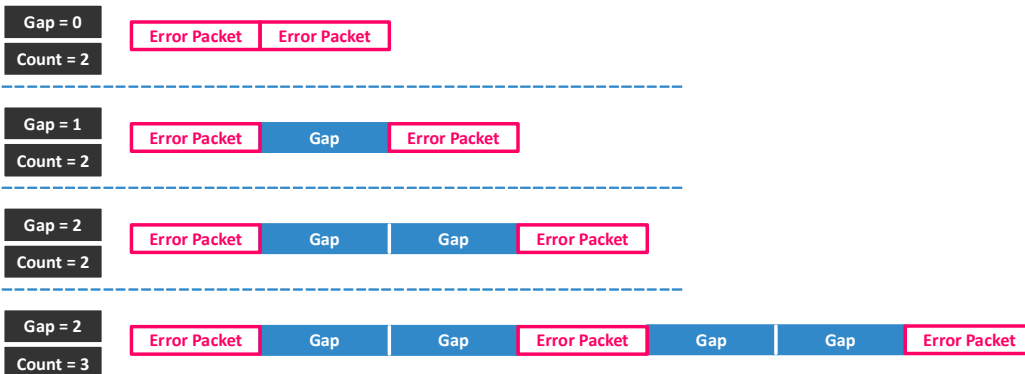
Error Injection Control Panel

6. Select the Amount.

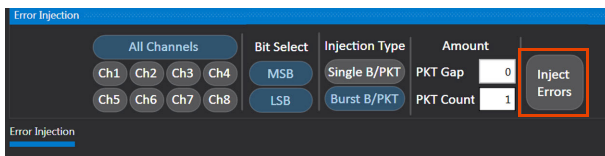


PKT Gap is the gap size between Error Packets; gap unit length is 64-symbols long.

PKT Count is the total number of Error Packets; packet unit length is 64-symbols long.



7. Click the **Inject Errors** button to generate errors.

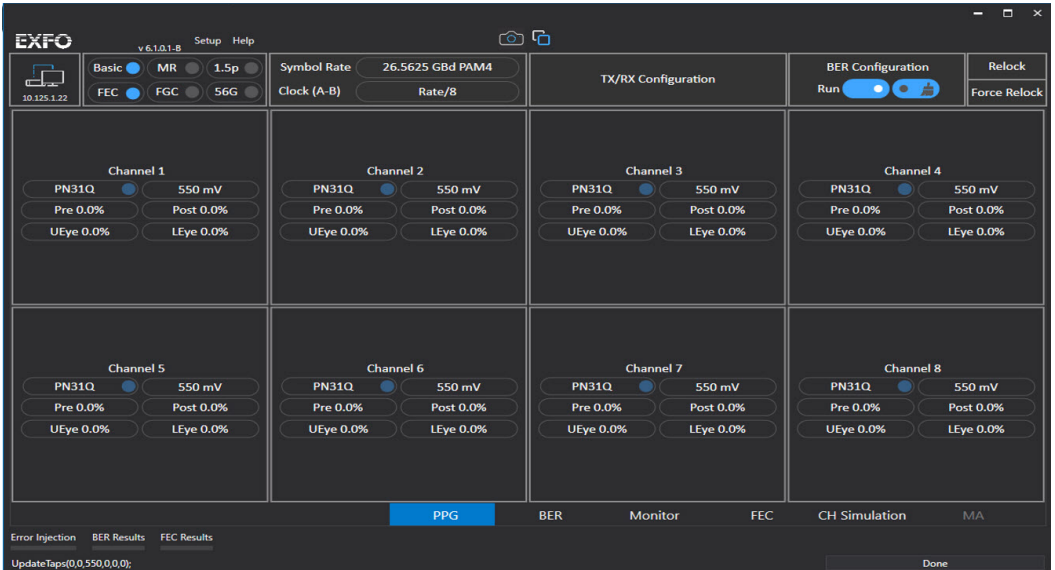
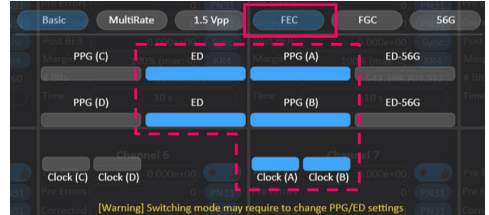


5 FEC Operation

FEC BER Page

To set and switch to the FEC BER page:

1. From the main control page, in the function mode area, select **FEC**.
2. Set the **Modulation** and **Symbol Rate**.
3. Set **TX/RX Configuration**.
4. Set BER test method.

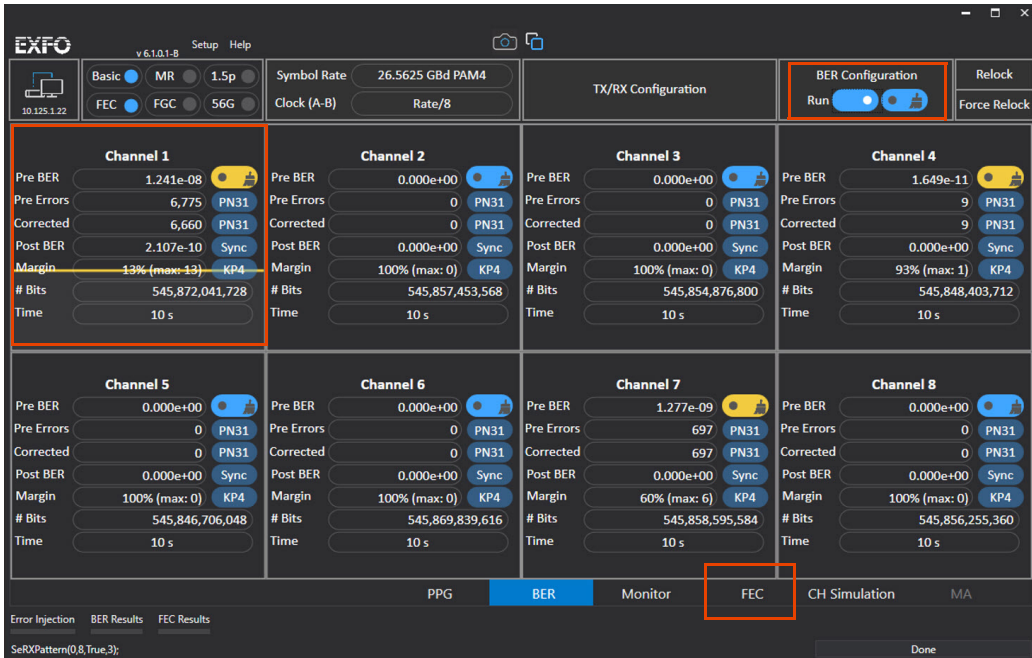


5. Click **BER** tab to display the FEC BER page.

FEC Operation

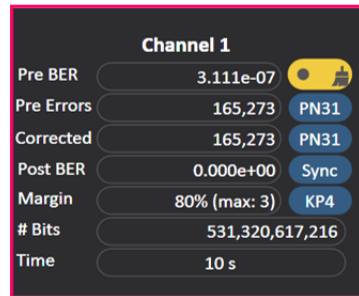
FEC BER Page

6. Start/stop BER test with FEC.




The FEC BER page lists before/after FEC information for all channels.

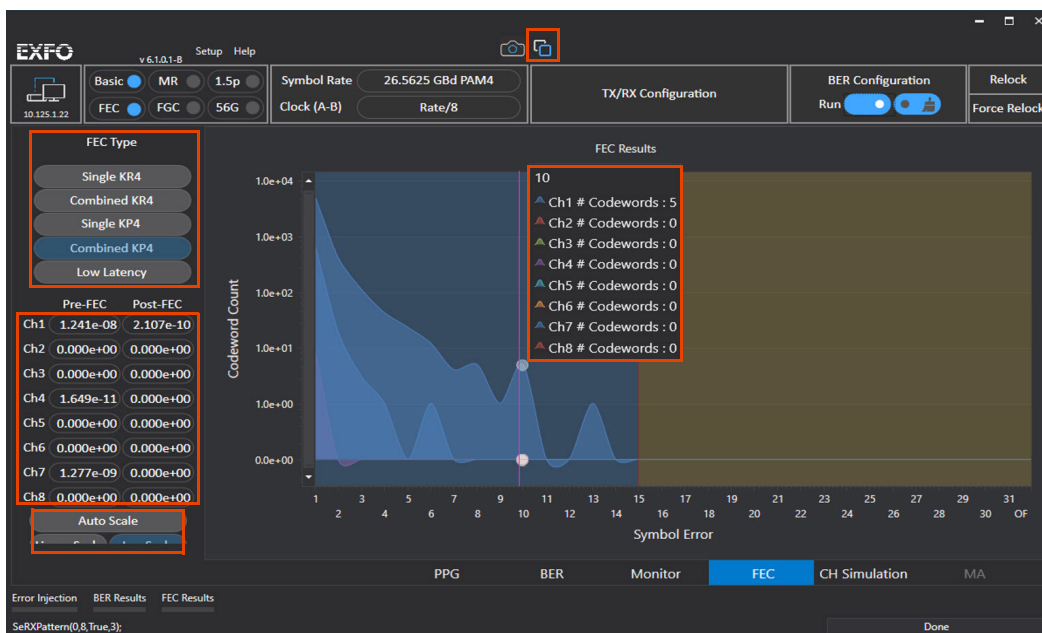
- **Pre BER:** Pre-FEC BER
- **Pre Errors:** Pre-FEC Bit Errors
- **Corrected** Bits by FEC
- **Post BER:** Post-FEC BER
- **FEC Margin**
- **# Bits:** Total test Bits



7. Click the **FEC** tab to show the FEC Plot page.

FEC Plot Page

This page displays the FEC plot of Symbol Errors per Codeword vs. **Codeword Count** depicting the behavior of error distribution. The full table of symbol error distribution can be copied by clicking .



- FEC Type allows you to set the type of FEC to **Single/Combined KR4/KP4**. Default is **Combined KP4**. Combined means striping to 4 channels.
- **Pre/Post-FEC BER** is displayed for each channel.
- The vertical axis scale can be set to Auto, Linear, or Log (Logarithmic).

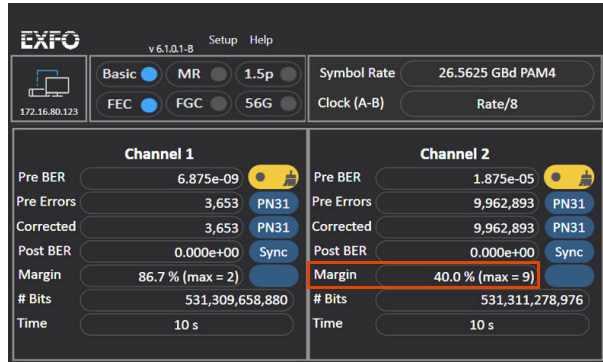
FEC Operation

FEC Plot Page

- In the **FEC Results**, move your mouse over the plot area to list the number of codewords with the amount of symbol errors. For example, in the above graphic, each codeword has **10** symbol errors with **CH1** having **5 Codewords**.
- Mouse controls:
 - Scroll to zoom in/out.
 - Drag up/down to move focus.
 - On the keyboard [Shift] + drag mouse down to zoom in the area.

FEC Margin and Log Scale

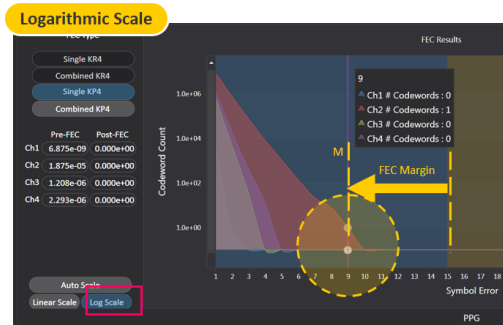
FEC **Margin** indicates how much margin is required to keep error symbols correctable.



For KP4, it is defined as shown on the right, where M is the **max** (that is, maximum symbol errors per codeword).

$$\text{FEC margin} = \frac{15 - M}{15} \times 100\%$$

Switching from **Linear Scale** to **Log Scale** to show obvious minor errors makes it easier to identify the maximum symbol errors per codeword and FEC margin.



FEC Operation

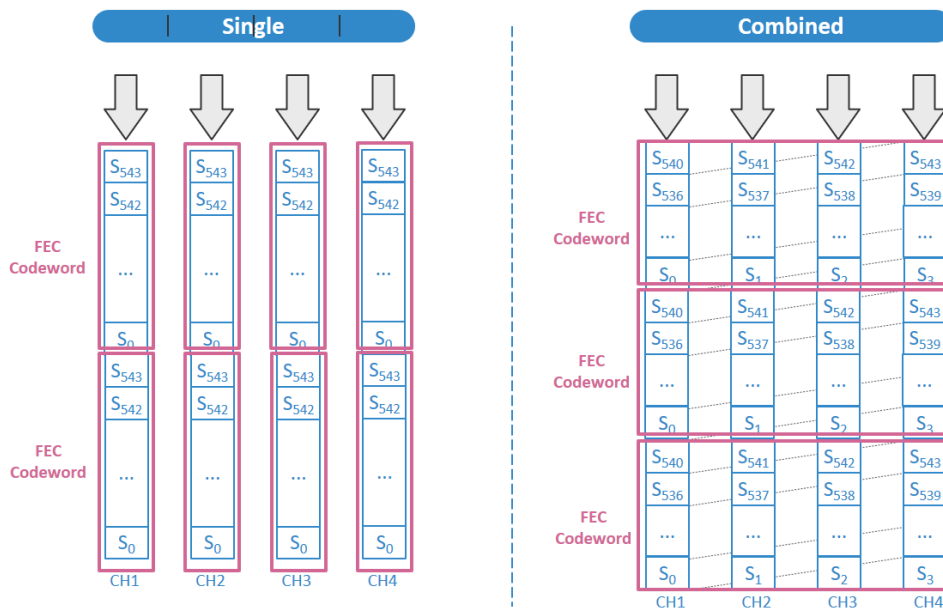
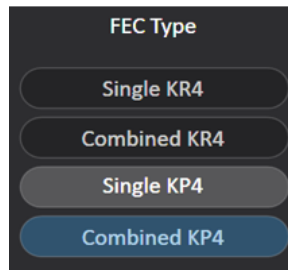
FEC Type

FEC Type

KR4 means KR4 RS-FEC. That is, RS(528, 514).

KP4 means KP4 RS-FEC. That is, RS(544, 514).

- **Single** calculates **FEC Codeword** by individual CH (channel).
- **Combined** calculates **FEC Codeword** by combining 4 channels.



Example of Single and Combined FEC

➤ Single KP4

Channel 1		Channel 2		Channel 3		Channel 4	
Pre BER	4.946e-07	Pre BER	9.867e-04	Pre BER	1.300e-08	Pre BER	4.569e-05
Pre Errors	262,800	Pre Errors	524,277,216	Pre Errors	6,906	Pre Errors	24,276,209
Corrected	258,809	Corrected	95,785,166	Corrected	6,906	Corrected	21,112,443
Post BER	7.511e-09	Post BER	8.065e-04	Post BER	0.000e+00	Post BER	5.955e-06
# Bits	531,323,521,280	# Bits	531,323,850,496	# Bits	531,323,627,648	# Bits	531,320,604,672
Time	10 s	Time	10 s	Time	10 s	Time	10 s

➤ Post-FEC BER

7.5×10^{-9}



Error Free

8.0×10^{-4}



4.7×10^{-4}

Error Free



Error Free

5.9×10^{-6}



1.1×10^{-6}

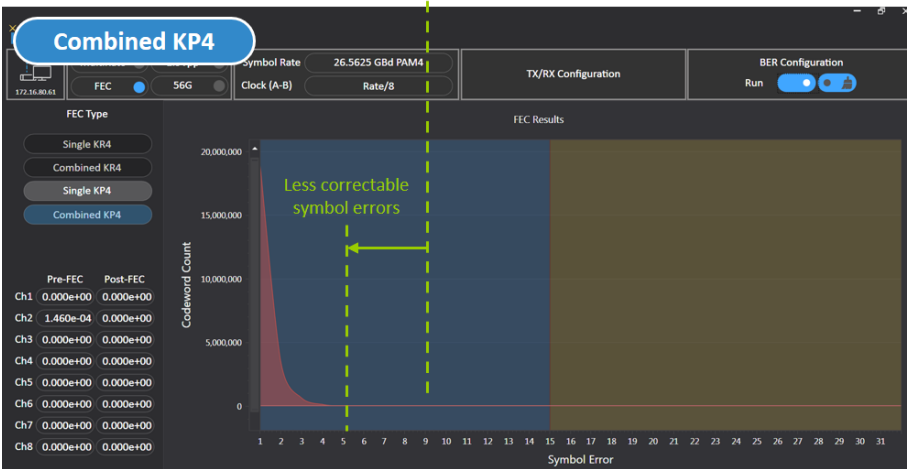
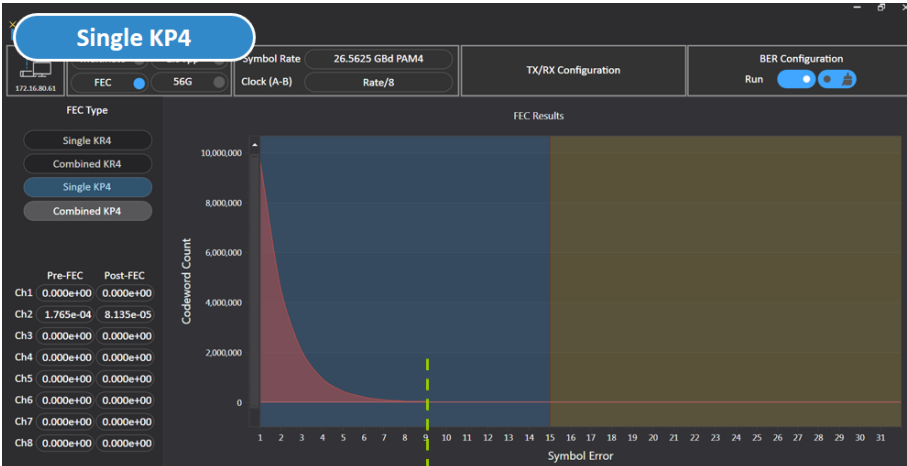
➤ Combined KP4

Channel 1		Channel 2		Channel 3		Channel 4	
Pre BER	3.784e-07	Pre BER	9.785e-04	Pre BER	1.605e-08	Pre BER	4.349e-05
Pre Errors	214,562	Pre Errors	561,325,978	Pre Errors	9,316	Pre Errors	25,532,810
Corrected	214,562	Corrected	287,824,421	Corrected	9,316	Corrected	24,839,112
Post BER	0.000e+00	Post BER	4.768e-04	Post BER	0.000e+00	Post BER	1.182e-06
# Bits	567,015,950,592	# Bits	573,657,540,096	# Bits	580,431,926,528	# Bits	587,114,560,640
Time	11 s	Time	11 s	Time	11 s	Time	11 s

FEC Operation

FEC Type

Example of Single and Combined FEC Cont'd



A **Assembly Guide**



IMPORTANT

Before assembly and disassembly, turn OFF power.



IMPORTANT

Before assembly, keep foreign body (for example, particles) from the mother board.



IMPORTANT

Always use the electric screwdriver provided.

Electric Screwdriver

Tune torsion of the screwdriver to 3.5.

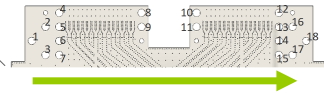
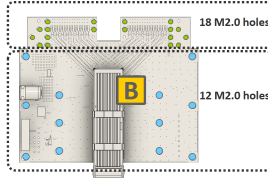


Assembly Guide

Assembly/Disassembly

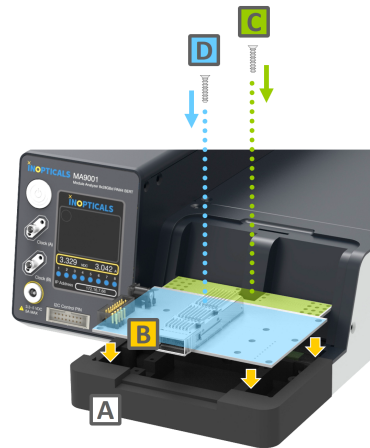
Assembly/Disassembly

	Item	Qty
A	MA with Board Holder	1
B	Module Test Board	1
C	M2.0 Screw	18
D	M2.0 Screw	12



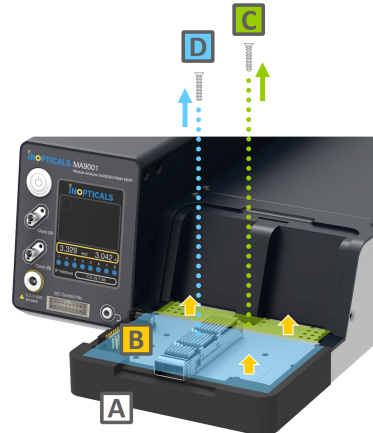
To assemble the MA:

1. Attach board [B] to holder [A].
2. Tighten the 18 screws [C] from left to right, as shown in the graphic above, right-hand side.
3. Tighten the 12 screws [D].



To disassemble the MA:

1. Remove the 12 screws [D].
2. Remove the 18 screws [C] from left to right, as shown in the top graphic, right-hand side.



B *Air Tube Joint*

Joint for Dry Air Supply



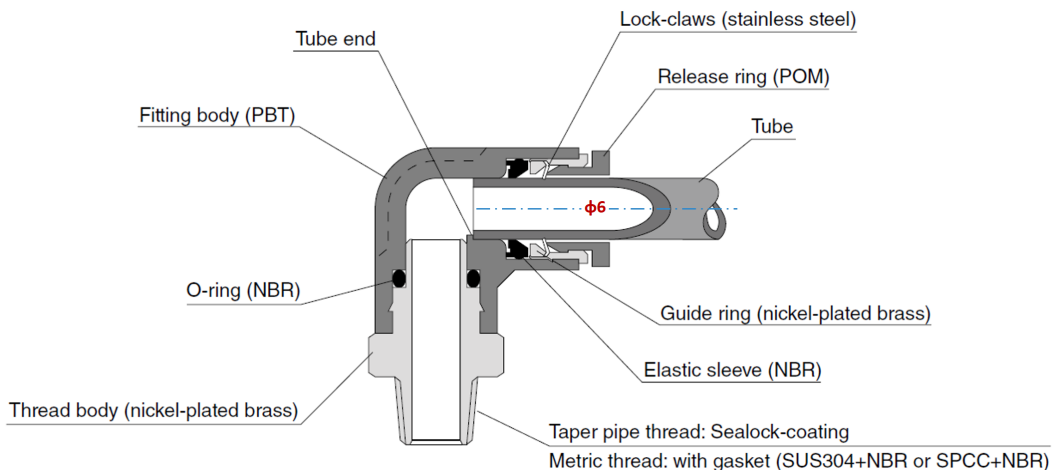
Dry air flow removes water vapor to prevent any condensation from the module test board.

A thermal stream provides pure dry air when connecting a tube to supply it.

Air Tube Joint

Joint Specifications

Joint Specifications



Tube Fitting Standard Joint

- Tube diameter = $\phi 6$ mm
- Operating pressure = up to 1.0 MPa
- Operating temperature range = 0 to 60°C (no freezing)

Model is PC6-M6.

For further details, please visit:

<https://en.pisco.co.jp/product/detail/a/a01/>



C Self Test

Configuration

It is important to know if the MA performs well after assembly of the module test board. Please use an official loopback board to help check, and follow the method below.

Hardware

- MA-4000 All-in-One 8x28G PAM4 BERT
- MA-QSFPDD QSFP-DD Module Test Board
- LB-QSDD QSFP-DD Loopback Board

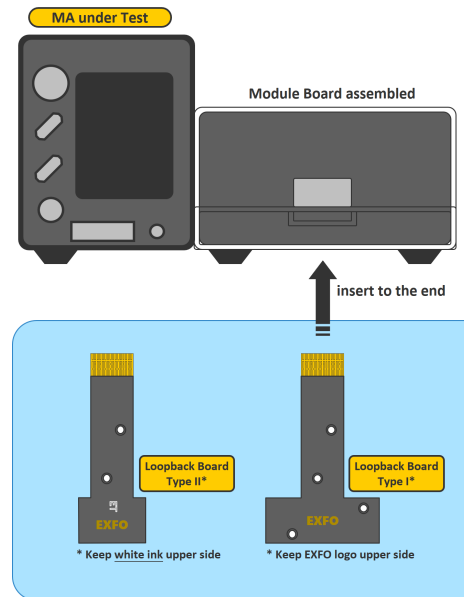
MA Settings

- Modulation: PAM4
- Symbol Rate: 26.5625 GBd
- Pattern: PRBS31Q
- Amplitude 400 mV
- Pre-/Post-Cursor: 0
- Upper/Lower Eye: 0
- RX Sensitivity: Optimized
- CTLE: 2 dB

To run the self test:

1. Insert the loopback board to the end of the module test board connector on the MA.
2. Test 10-second BER.

Criteria: ALL CH's BER < 1×10^{-9}



Self Test

Example of Self Test Results

Example of Self Test Results

The screenshot displays the INOPTICALs v3.12.1 interface. At the top, there are menu options (Setup, Help) and a status bar (172.16.98.18). The main configuration area includes:

- MultiRate:** 1.5Vpp
- FEC:** 56G
- Symbol Rate:** 26.5625 Gbd PAM4
- Clock (C-D):** Rate/8
- TX/RX Configuration:** (Empty)
- BER Configuration:** Run
- Relock:** Force Relock

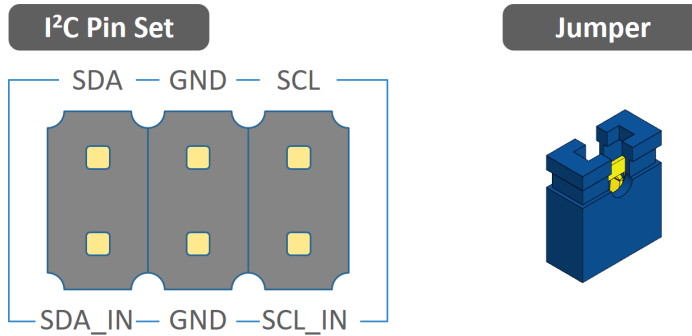
The main area is divided into 8 channel panels, each showing the following metrics:

Channel	BER	Total Errors	MSB Errors	LSB Errors	# Bits	Time
Channel 1	4.140e-10	224	2	222	541,070,923,904	10 s
Channel 2	8.056e-10	436	7	429	541,181,058,560	10 s
Channel 3	0.000e+00	0	0	0	541,289,466,880	10 s
Channel 4	0.000e+00	0	0	0	541,399,962,752	10 s
Channel 5	0.000e+00	0	0	0	541,512,004,608	10 s
Channel 6	3.416e-10	185	0	185	541,623,106,432	10 s
Channel 7	6.664e-10	361	11	350	541,735,424,384	10 s
Channel 8	9.228e-12	5	2	3	541,847,631,104	10 s

At the bottom, there is a navigation bar with tabs: PPG, **BER**, Monitor, FEC, CH Simulation, MA. Below the navigation bar, it shows 'Error Injection: BER Results' and 'UpdateTaps(0,0,400,0,0): 3.376 V 0.020 A Done'.

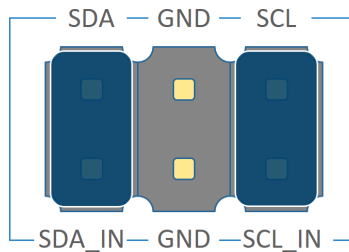
D Accessing I²C

On the module test board, there is an I²C pin set.



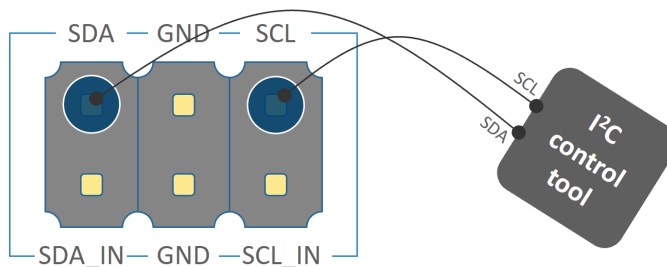
To access I²C signal via the MA:

Insert the 2 jumpers connecting **SDA** to **SDA_IN** and **SCL** to **SCL_IN**.



To access I²C signal by an external tool:

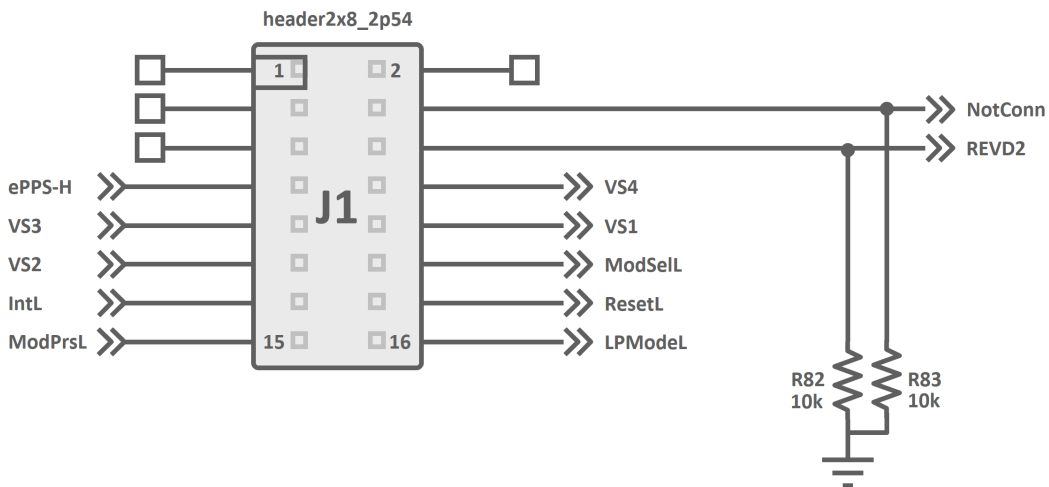
Remove the jumpers, and connect **SDA** and **SCL** to the tool.



E Module Test Board Schematics

New Module Test Board MA-QSFPDD

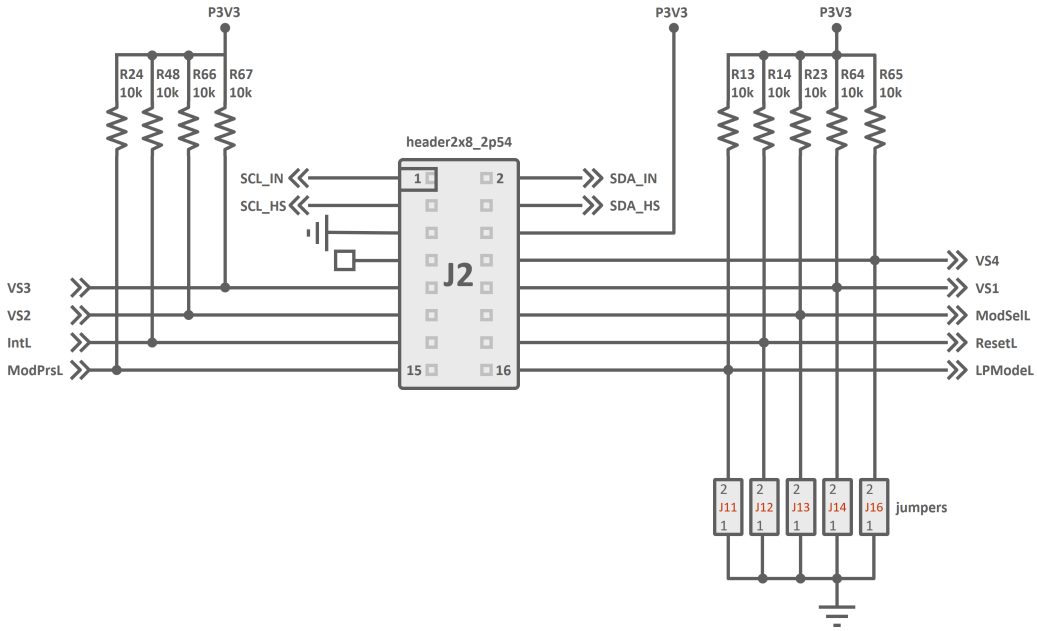
J1



Module Test Board Schematics

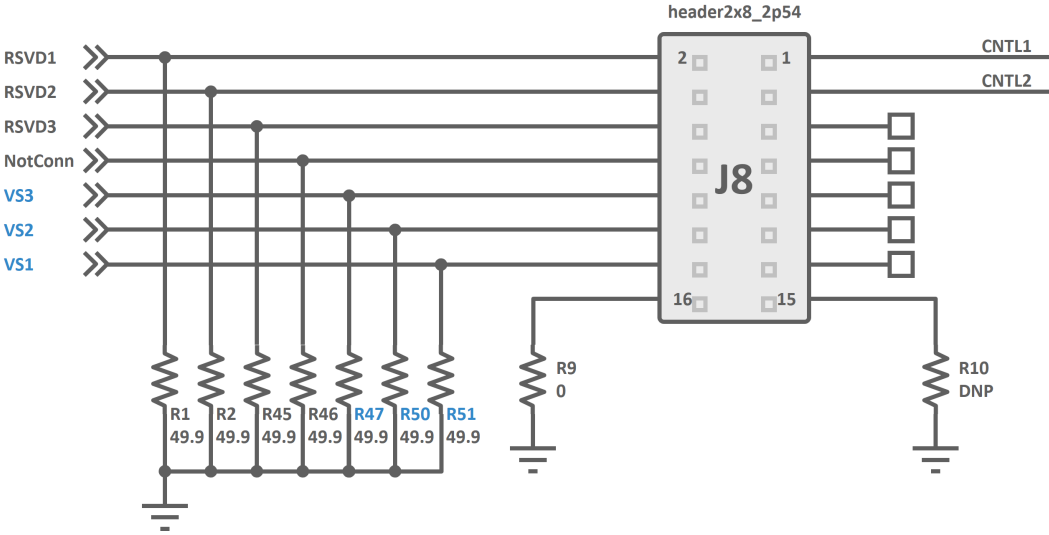
New Module Test Board MA-QSFPDD

J2



Module Test Board MA2856 (QSFP-DD)

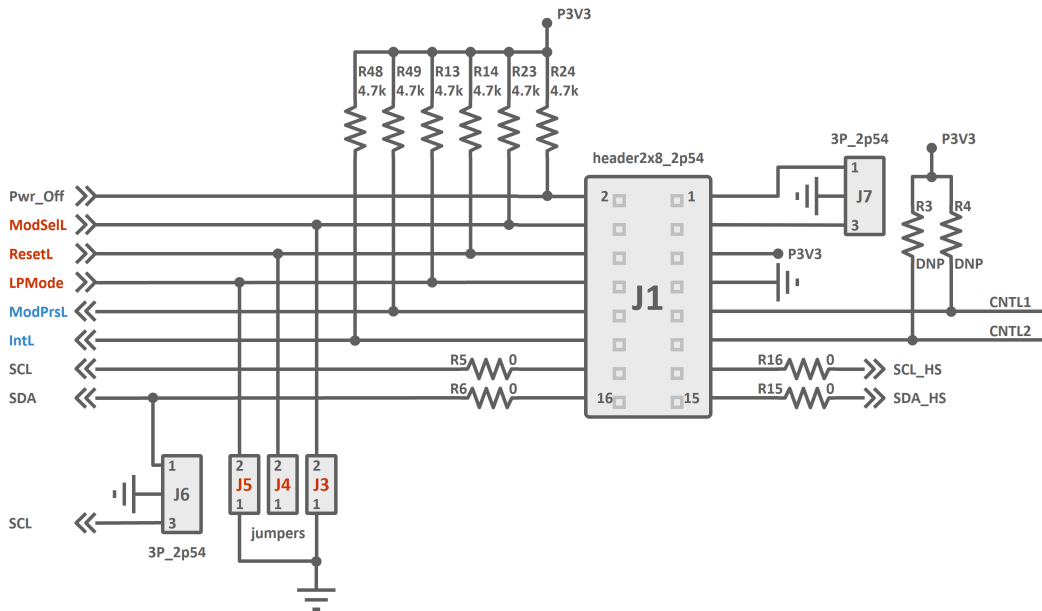
VS1/VS2/VS3



Module Test Board Schematics

Module Test Board MA2856 (QSFP-DD)

Low Speed Electrical Hardware Signals



F Setup IP on Control PC

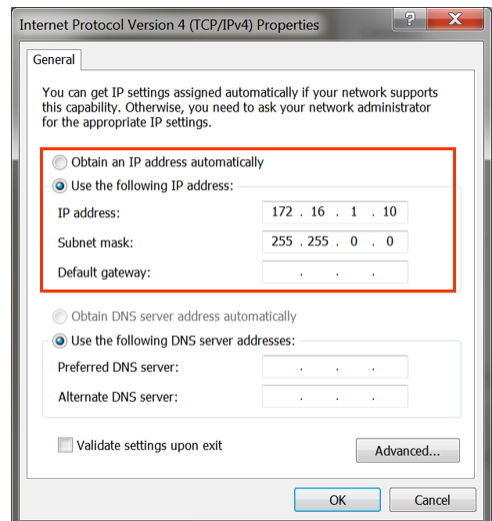
Quick Guide to Set IP Address

The IP address of the unit is 172.16.80.xxx (for example, 172.16.80.51). Therefore, set the IP Address of control PC as 172.16.yyy.zzz (for example, 172.16.1.1) and set the Subnet Mask as 255.255.0.0.



To set the IP address:

1. Open **TCP/IPv4 Properties** of the connected Ethernet device.
2. Select **Use the following IP address:**
3. Type **IP address** as **172.16.1.10**.
4. Type **Subnet mask** as **255.255.0.0**.




Setup IP on Control PC

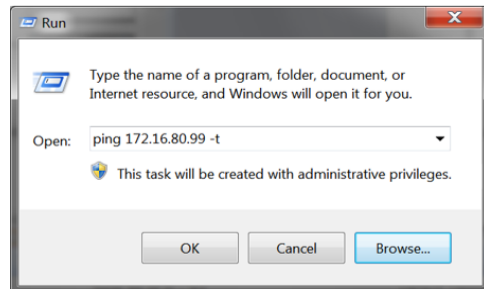
Pinging the Unit

Pinging the Unit

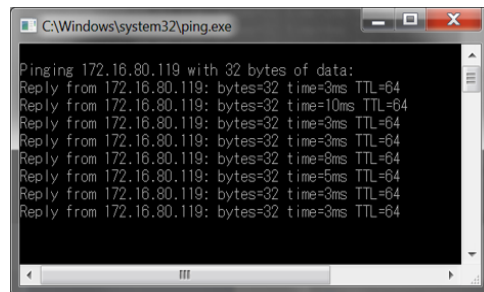
In order to check that the IP settings are correct, you can ping the unit. Getting a reply under 3 ms means the connection is correct. Otherwise, something is wrong.

To ping the unit:

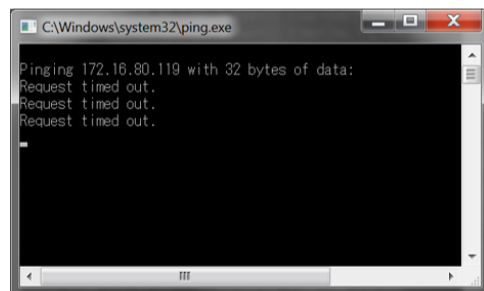
1. On your keyboard, click  [Win] + [R] to open the Command Prompt.
2. Type the command **ping 172.16.80.99 -t**.
3. Click **OK**.



If well connected, this screen is displayed.




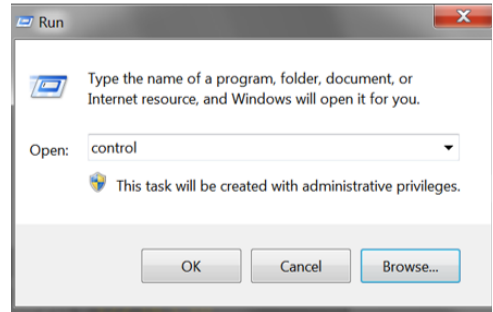
If disconnected, this screen is displayed.



Accessing the Control Panel in Windows

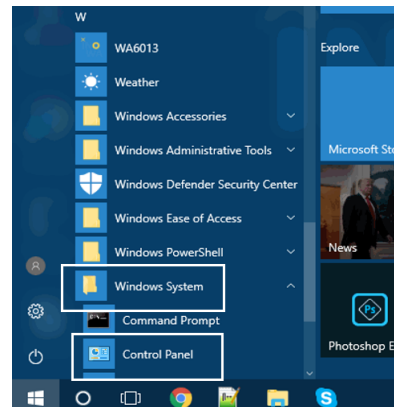
To open the control panel in Windows 7 and 10:

1. On your keyboard, click  [Win] + [R] to open the Command Prompt.
2. Type **control** in the **Open** field.
3. Click **OK**.



To open the control panel in Windows 10 only:

1. Expand the Start menu.
2. Select **Windows System** folder.
3. Select **Control Panel**.



Note: The supported Operating Systems are Microsoft Windows 7 SP1 (x86 and x64) and Microsoft Windows 10 (x86 and x64).

Note: The GUI requires .NET Framework 4.6.1 to work. It is Microsoft official resource. The link is below:

<https://dotnet.microsoft.com/download/thank-you/net461or>

<https://www.microsoft.com/en-us/download/details.aspx?id=49982>

Setup IP on Control PC

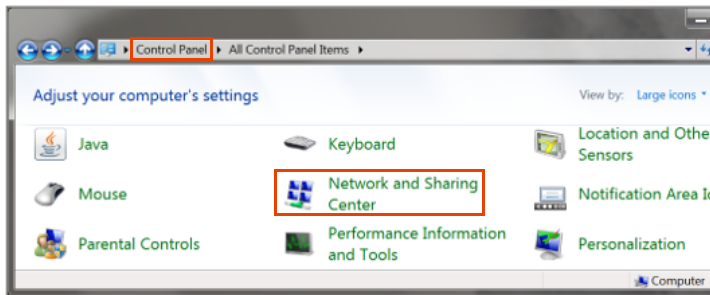
Setting the IP Address in Windows 7 and 10

Setting the IP Address in Windows 7 and 10

The procedure is the same for both Windows 7 and 10. Windows 7 screen shots are used as examples.

To set the IP address:

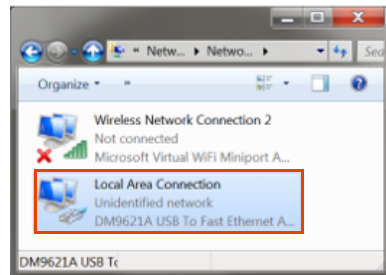
1. Open the **Control Panel** and enter **Network and Sharing Center**.



2. Click **Change adapter settings**.



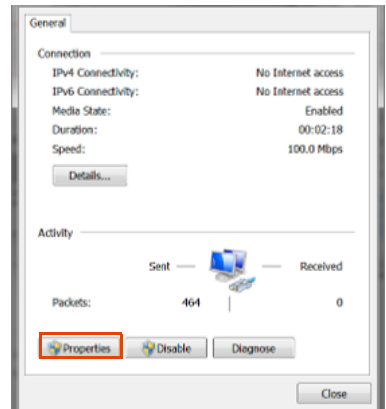
3. Select the Ethernet device already linked to the unit.



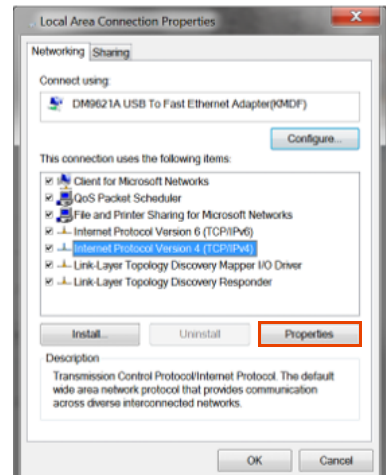
Setup IP on Control PC

Setting the IP Address in Windows 7 and 10

4. Click **Properties**.



5. Select **IPv4** and click **Properties**.



Setup IP on Control PC

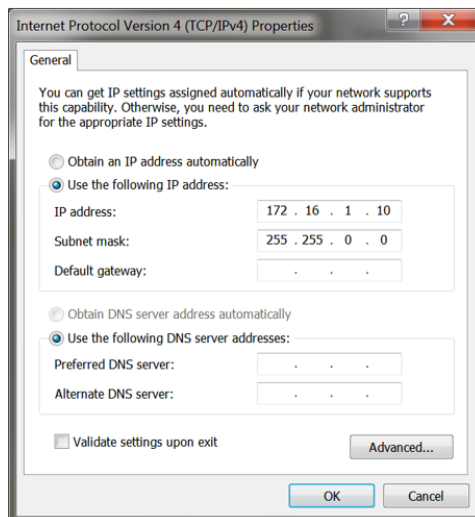
Setting the IP Address in Windows 7 and 10

6. Setup IP address by selecting **Use the following IP address:**

IP address = 172.16.1.10

Subnet mask = 255.255.0.0

7. Click **OK**.

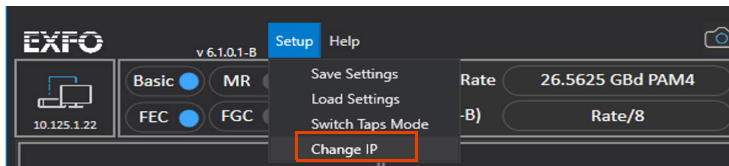


Changing the IP Address

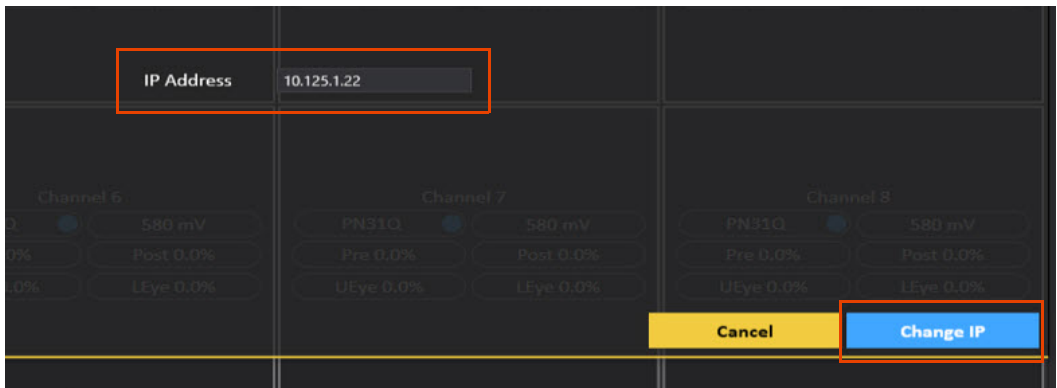
The tool of changing the unit's IP address is already integrated in the GUI.

To change the IP address of the unit:

1. Connect the unit.
2. Click **Change IP** in the **Setup** menu.



3. Input the desired **IP Address**.

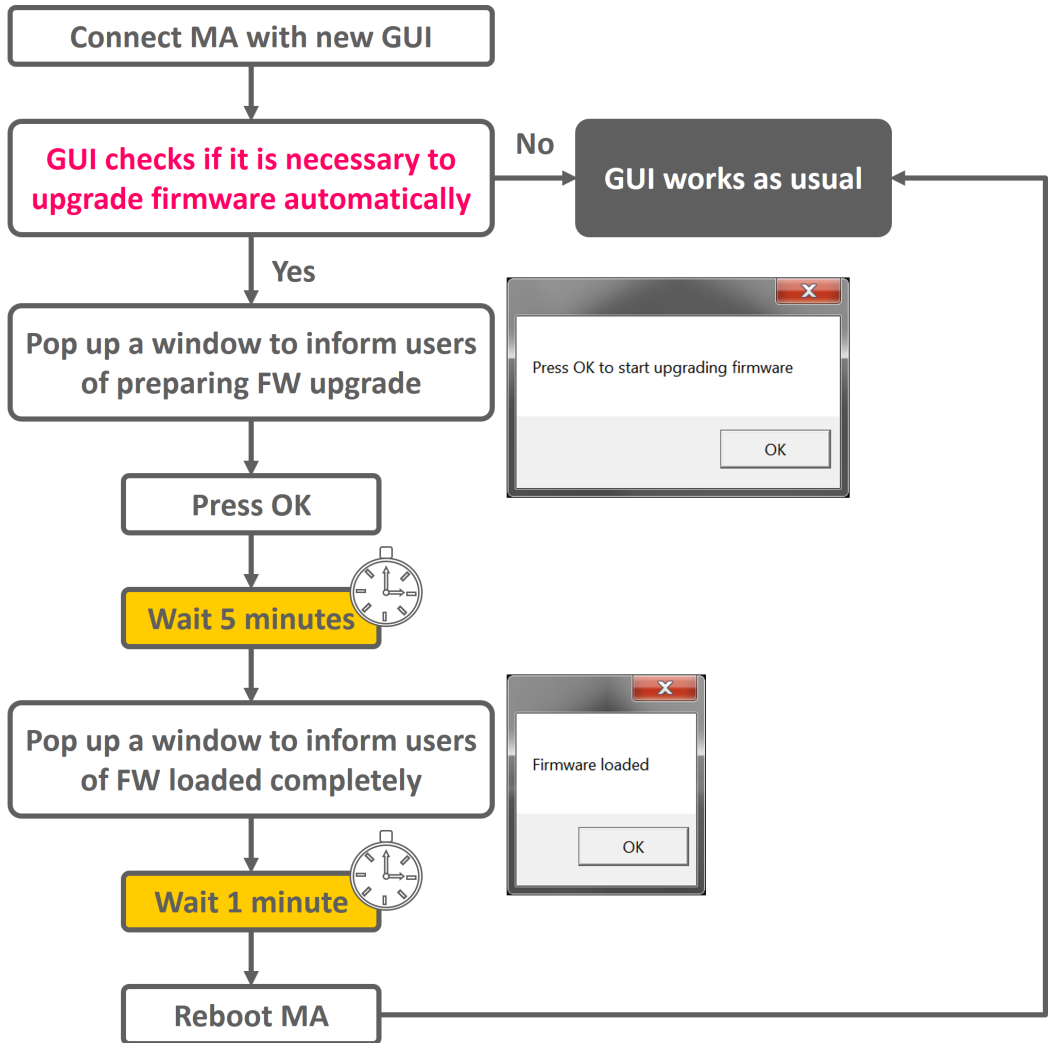


4. Click the **Change IP** button.
5. Wait 10 seconds and reboot the unit (IP is already changed).

To confirm if the IP was changed, ping the unit. If a reply is received, the address was changed successfully.

G **Firmware Upgrade and API Update**

You can download the latest GUI to upgrade and run the MA (Module Analyzer) with new functions. The upgrade process is displayed as follows.

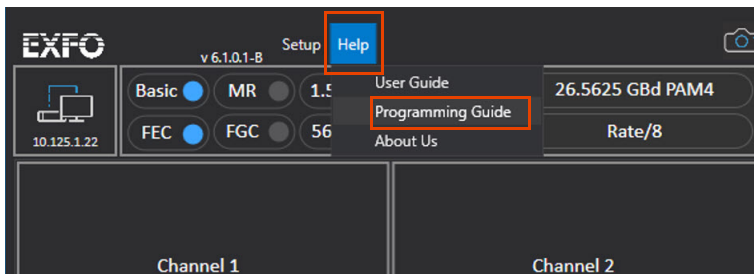


Downloading the API

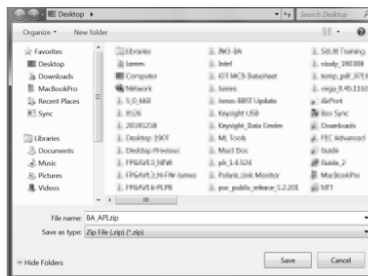
You can program and develop tools to control the MA by API. The API is downloadable from the GUI itself.

To download the API:

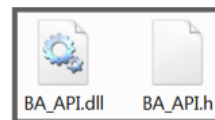
1. Click **Help** on the top bar then **Programming Guide**.



2. Save **MA_API.zip**.



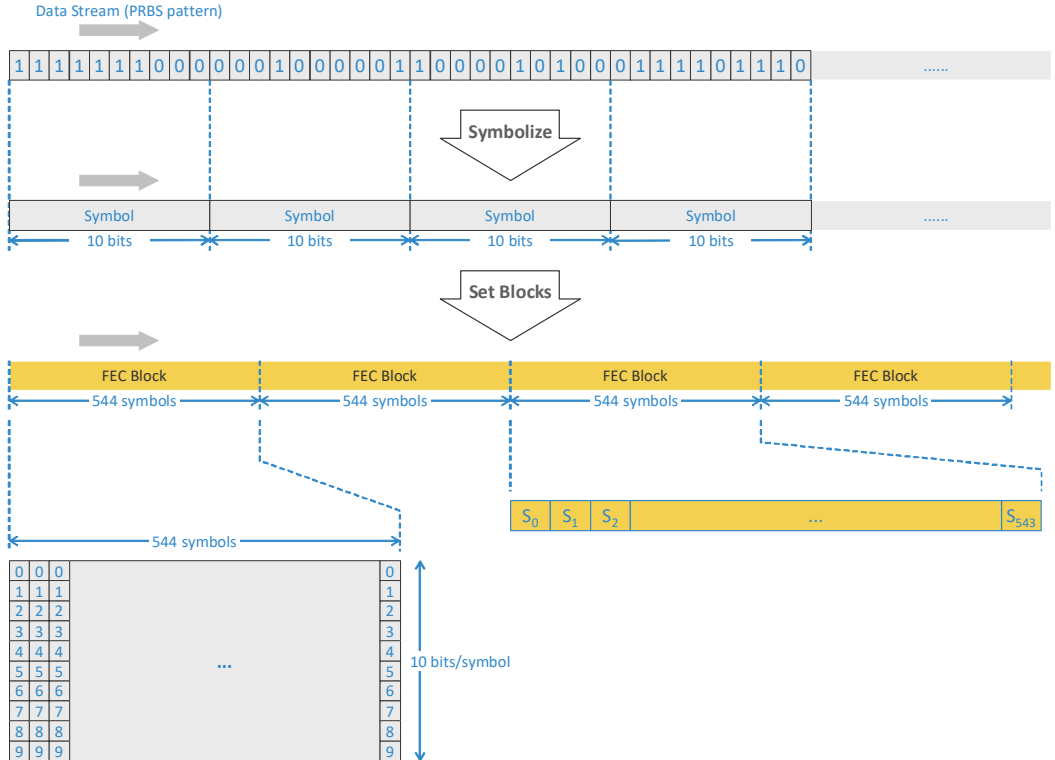
3. Extract **MA_API.dll** and **MA_API.h**.



H Structure of FEC Simulation

Symbol & Block

KP4 RS-FEC example:

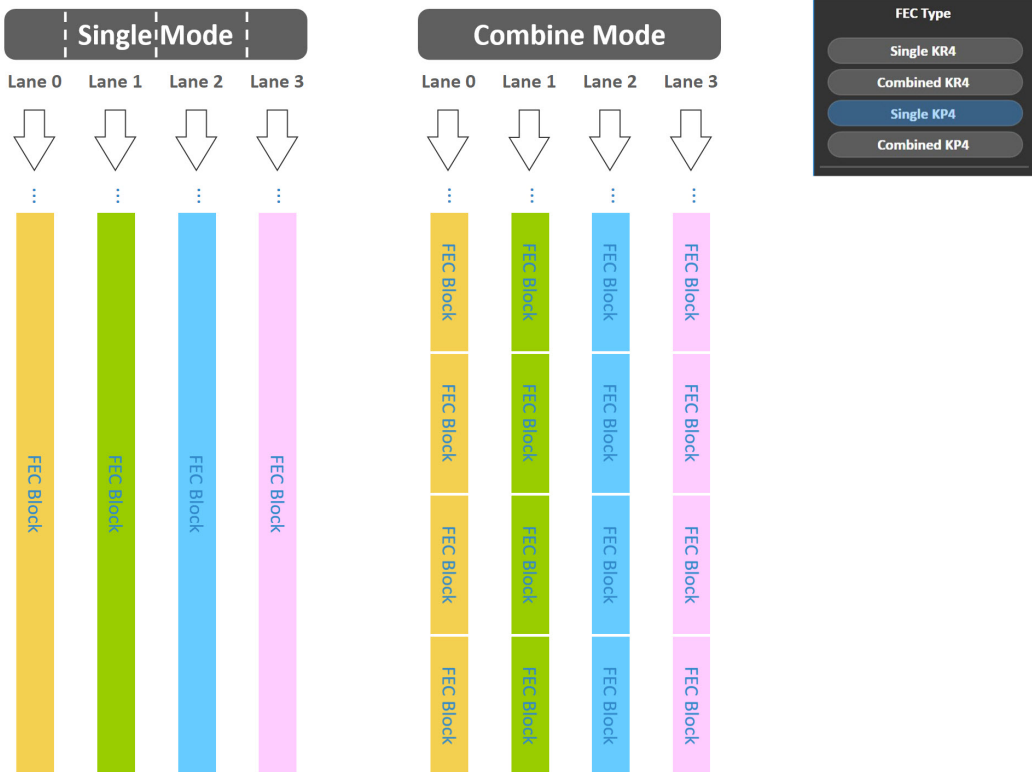


Structure of FEC Simulation

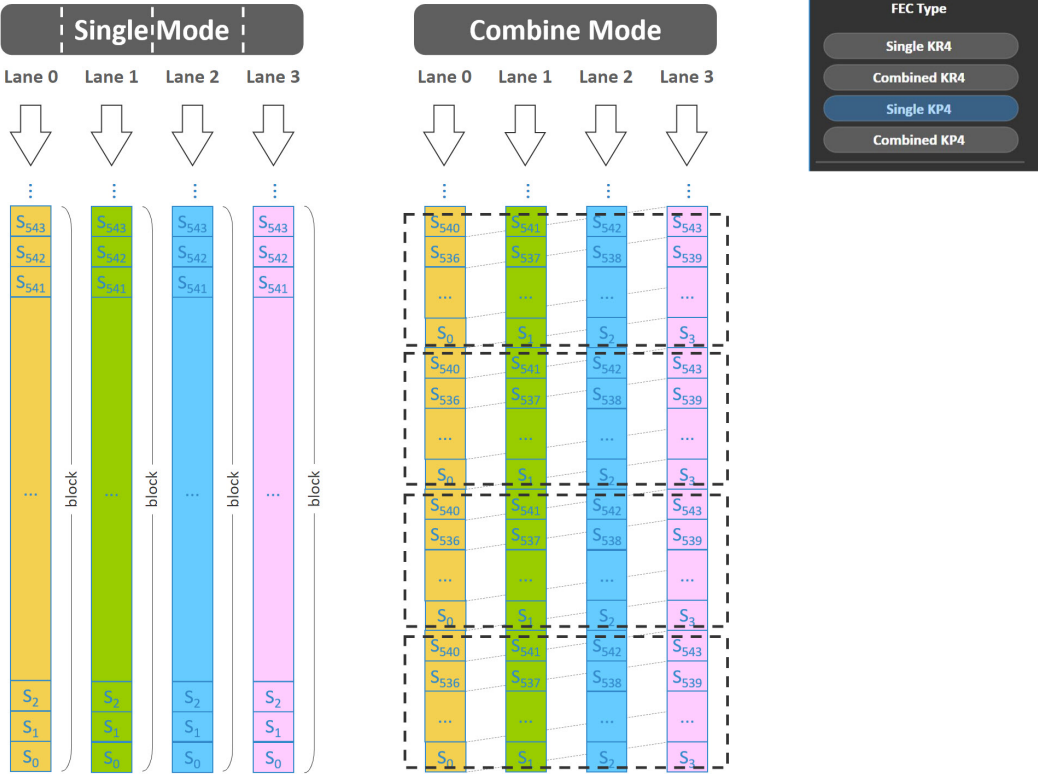
Striping

Striping

KP4 RS-FEC example:



Striping cont'd

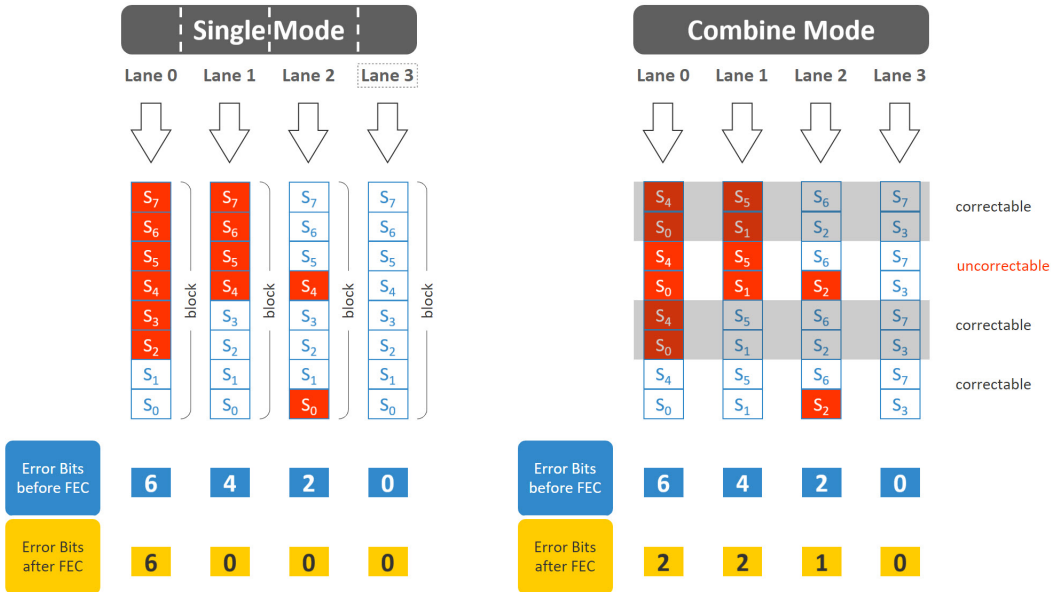


Structure of FEC Simulation

Striping

How Striping Works

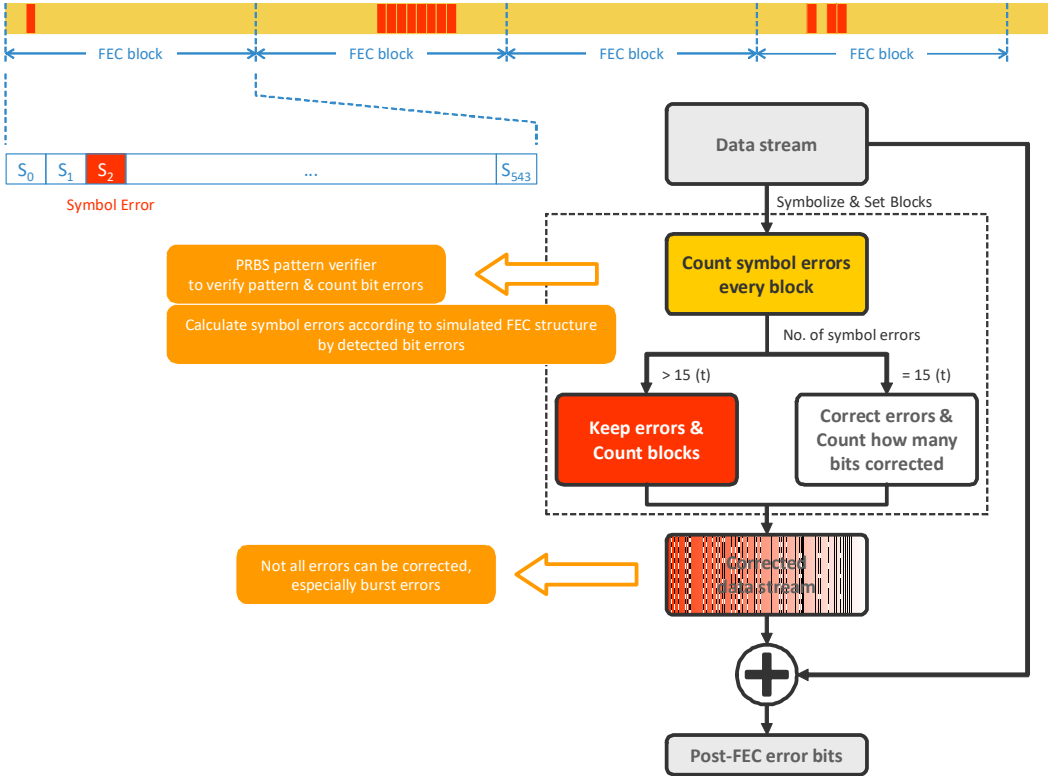
- Supposed
 - 8 Symbols = 1 Block
 - Max Correctable Symbols = 4



Flow Chart

KP4 RS-FEC example:

- Bits per symbol (m) = 10
- Total symbols (n) = 544
- Message symbols (k) = 514
- Parity symbols ($2t$) = 30
- Max correctable symbols (t) = 15



I **External Power Supply**

Power Barrel Connector Jack

2.50 mm ID (0.098") and 5.50 mm OD (0.217")



Power Plug

- CONN PWR PLUG 2.5X5.5MM SOLDER
- Power Barrel Connector Plug
 - 2.50 mm ID (0.098")
 - 5.50 mm OD (0.217") Free Hanging (In-Line)



<https://www.digikey.com/en/products/detail/cui-devices/PP3-002B/992137>

Cable Assembly

- CBL ASSEM R/A PLUG 2.5MM 18AWG
- Cable Assembly 2.5 mm ID, 5.5 mm OD Plug, Right Angle to Wire Leads Round 6.0' (1.83 m)
- Connector type:
 - 2.5 mm ID
 - 5.5 mm OD



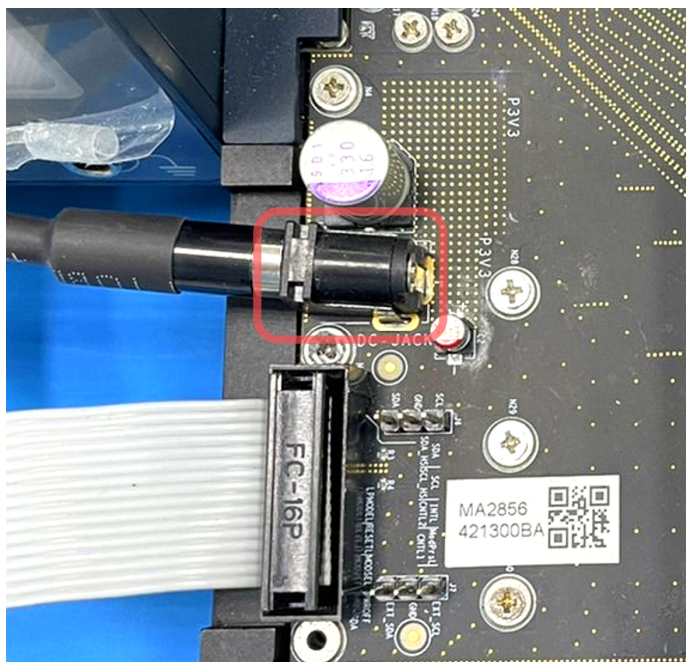
<https://www.digikey.com/en/products/detail/tensility-international-corp/10-02226/6412241>

External Power Supply

Cable Assembly

To provide external power supply to the MA module board:

Manually assemble a cable to the power barrel connector jack.



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P/N: 1.0.0.1

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